Introduction to Programmable Logic Devices

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Detector & Electronics Division

PPD Lectures

Programmable Logic is Key Underlying Technology.

- **First-Level and High-Level Triggering**
- **Data Transport**
- **Computers interacting with Hardware (VME Bus)**
- **Silicon Trackers (Reading out Millions of Data Channels)**

Commercial Devices. Developments driven by Industry.
Telecomms, Gaming, Aerospace, Automotive, Set-top boxes….

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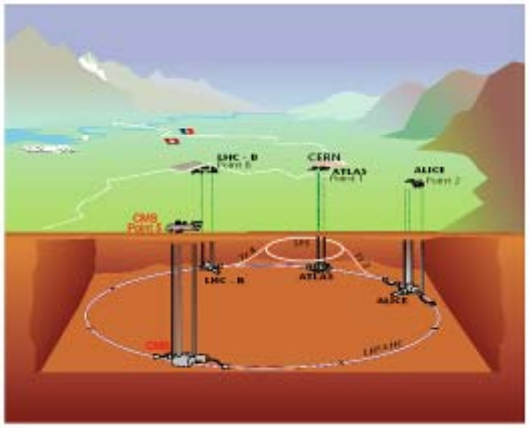
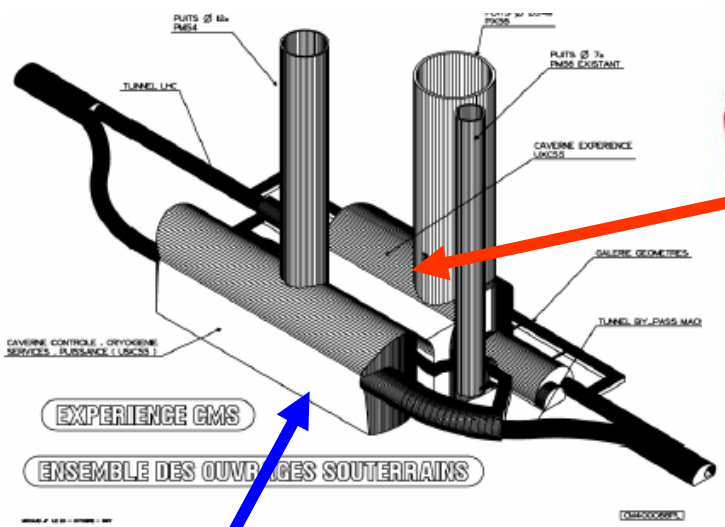
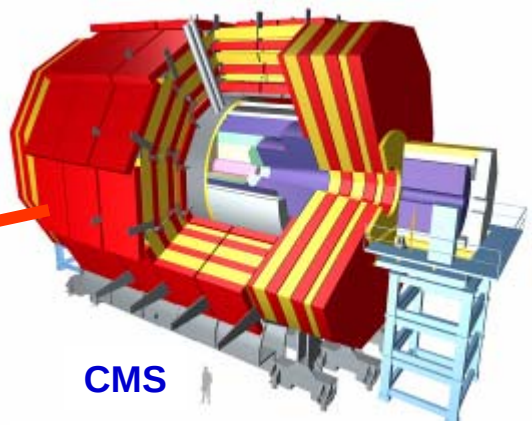
Particle Physics Electronics



CERN LHC



The underground area at point 5, showing the access shafts, the two large caverns and the wall between them



CMS

Custom Electronics Chips
ASICs
Rad Hard, Low Power

Electronics “Counting” Room(s)

Trigger Systems. DAQ Systems.

Purpose Built Digital Processing Boards
In VME Bus Crates

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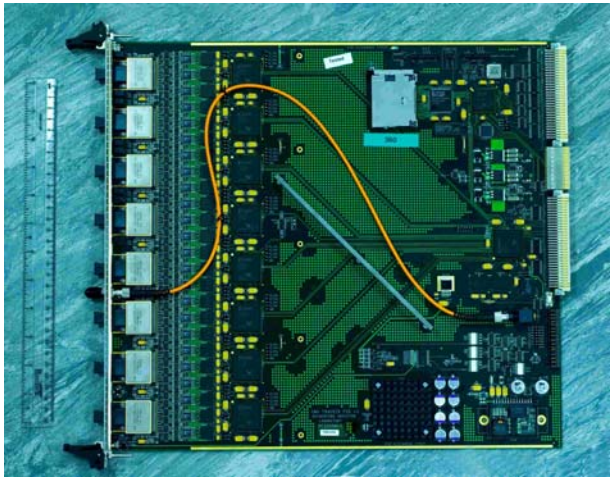
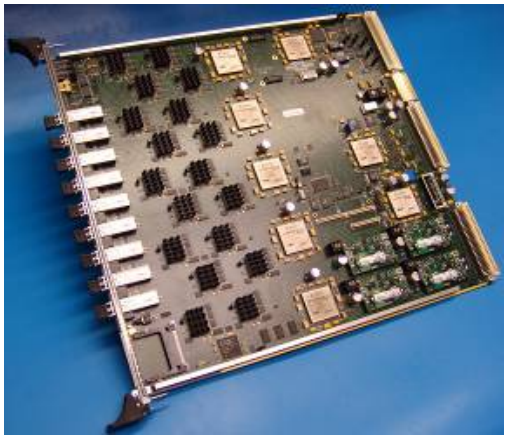
Particle Physics Electronics

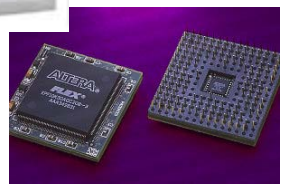
- **Special Dedicated Logic Functions (not possible in CPUs)**
  - **Ultra Fast Trigger Systems (Trigger Algorithms) Clock Accurate Timing**
  - **Massively Parallel Data Processing (Silicon Trackers with Millions of Channels)**

Custom Designed
Printed Circuit Boards PCBs.





Commercial
Programmable Logic Devices



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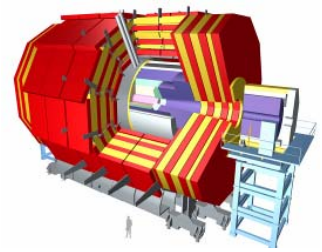
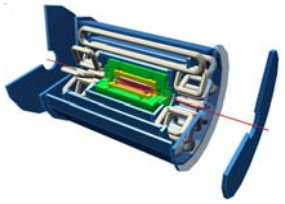
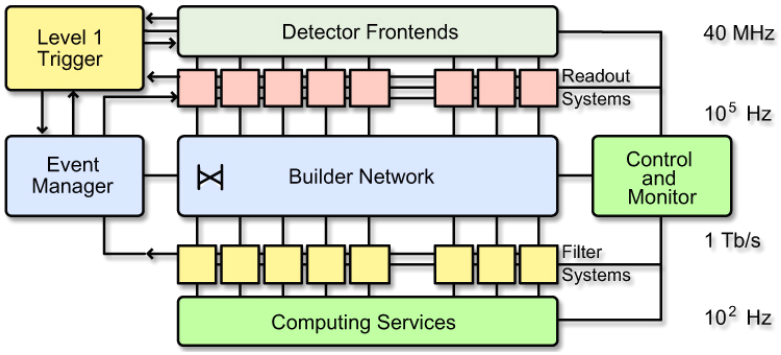
CMS & ATLAS DAQ/Trigger Architectures



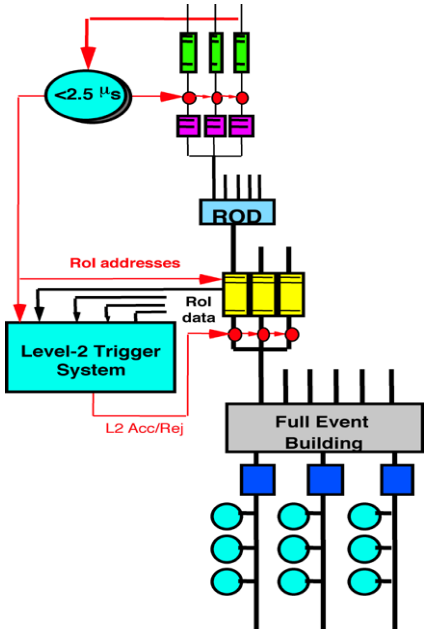
CMS



ATLAS



"Telecoms Network"



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Lecture Outline

- **Programmable Logic Devices**
  - **Basics**
  - **Evolution**
- **FPGA Field Programmable Gate Arrays**
  - **Architecture**
- **Design Flow**
  - **Design Tools**
  - **Hardware Description Languages**

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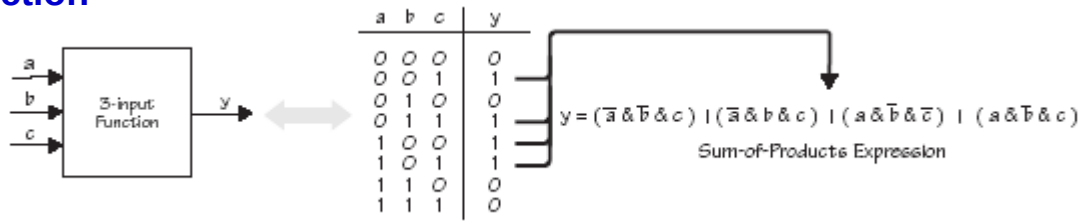
Digital Logic

Digital Logic Function

3 Inputs



Product AND (&)
Sum OR (|)

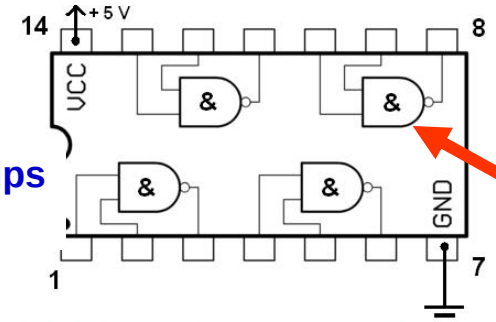
Black Box

Truth Table
(Look Up Table LUT)

SUM of PRODUCTS

Boolean Logic Minimisation

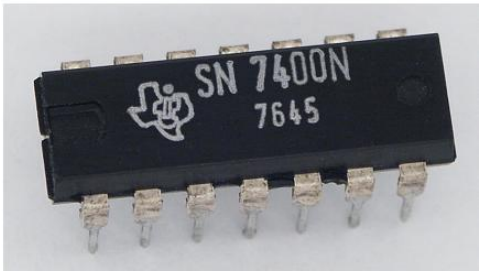
Connect Standard Logic Chips
Very Simple Glue Logic



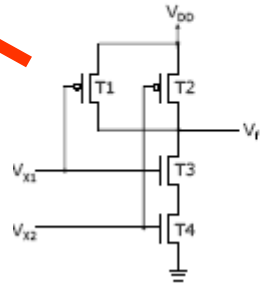
Discrete Logic

Large board area

FIXED Logic



CMOS NAND gate



X1	X2	T1	T2	T3	T4	f
0	0	On	On	Off	Off	1
0	1	On	Off	Off	On	1
1	0	Off	On	On	Off	1
1	1	Off	Off	On	On	0

Transistor Switches

MOORE'S LAW **40 nm!**

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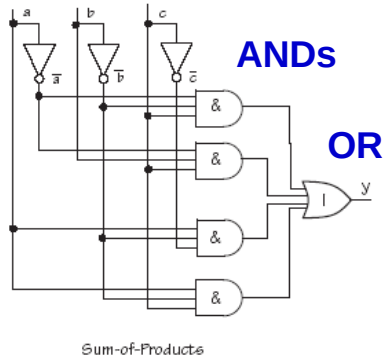
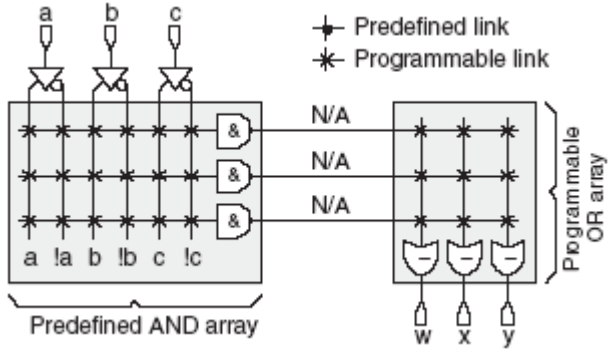
Programmable Logic Devices
PLDs

- **SUM of PRODUCTS**
- **(Re-)Programmble Links**
- **Reconfigurable**



Sum of Products

Inputs



Un-programmed State

Planes of ANDs, ORs

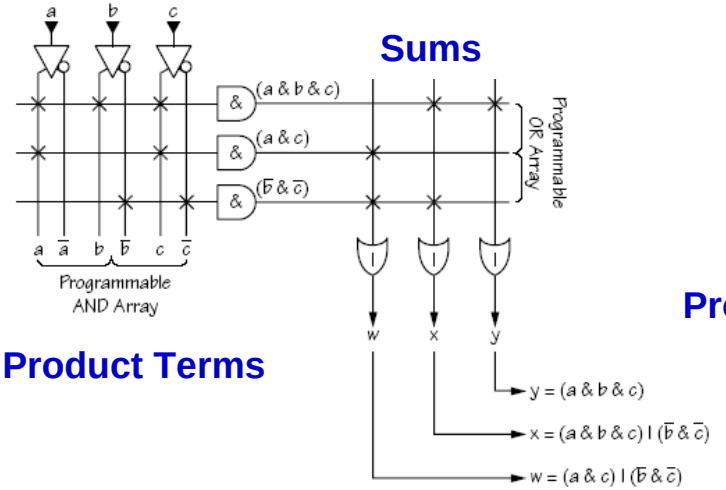
Outputs

$y = (a \,\&\, b \,\&\, c)$

$x = (a \,\&\, b \,\&\, c) \mid (\bar{b} \,\&\, \bar{c})$

$w = (a \,\&\, c) \mid (\bar{b} \,\&\, \bar{c})$

Logic Functions



Product Terms

Programmed PLD

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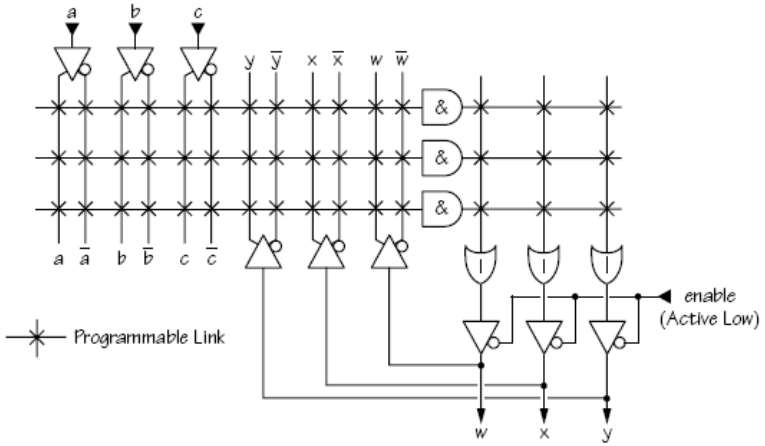
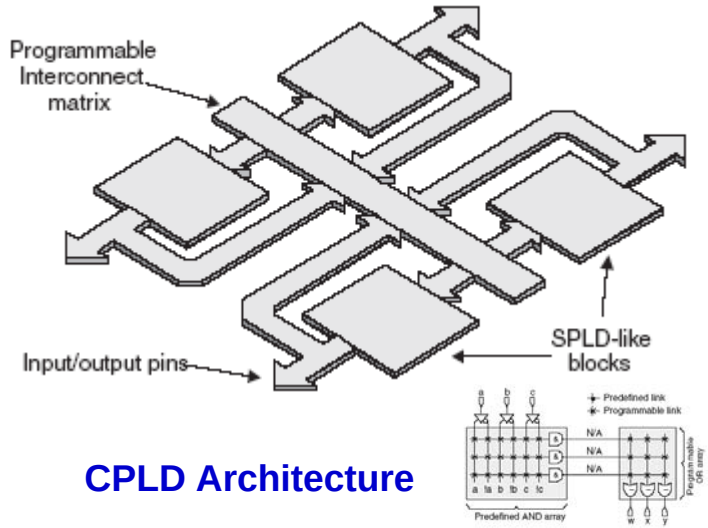
Complex PLDs

- **CPLDs**
- **Programmable PLD Blocks**
- **Programmable Interconnects**
- **Electrically Erasable links**



Feedback Outputs



CPLD Architecture

Add Flip Flops/Registers
(Clocked Logic) -> State Machines

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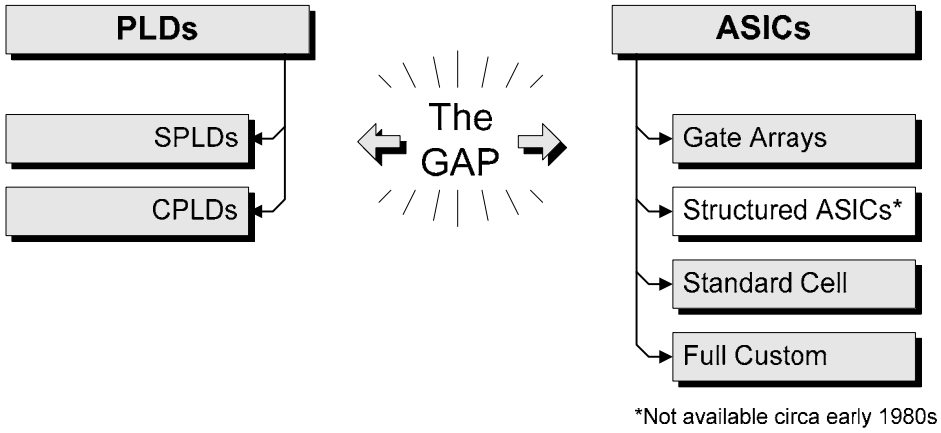
Application Specific Integrated Circuits ASICs

Prefabricated
Programmed



Custom Fabricated
Design from Scratch

Limited Complexity
Thousands of Gates

Large Complex Functions . Millions of Gates
Customised for Extremes of Speed, Low Power, Radiation Hardness

Cheap
Easy to Design
Reprogrammable.

(Very) Expensive to Design (in small quantities)
> $1 Million mask set
(Very) Hard to Design.
Long Design cycles.
NOT Reprogrammable. FROZEN in Silicon. High Risk

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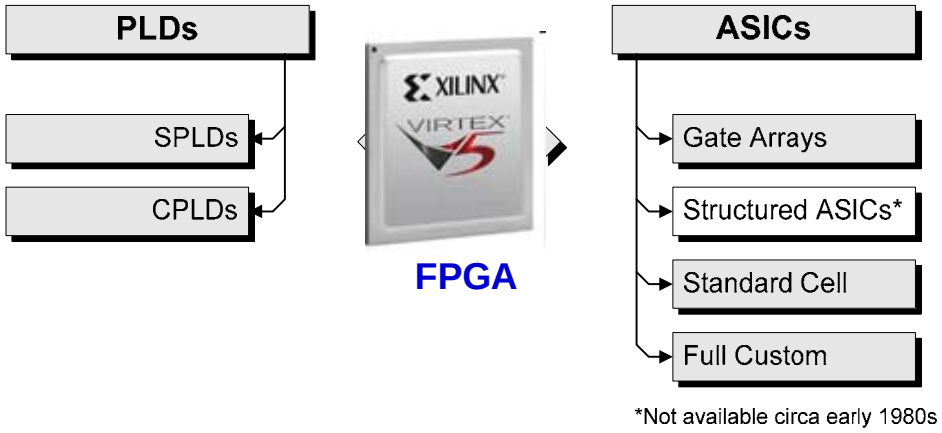
FPGAs



Large Complex Functions

Inexpensive
Easy to Design, Rapid Protoyping.
Reprogrammable. Changing data standards.

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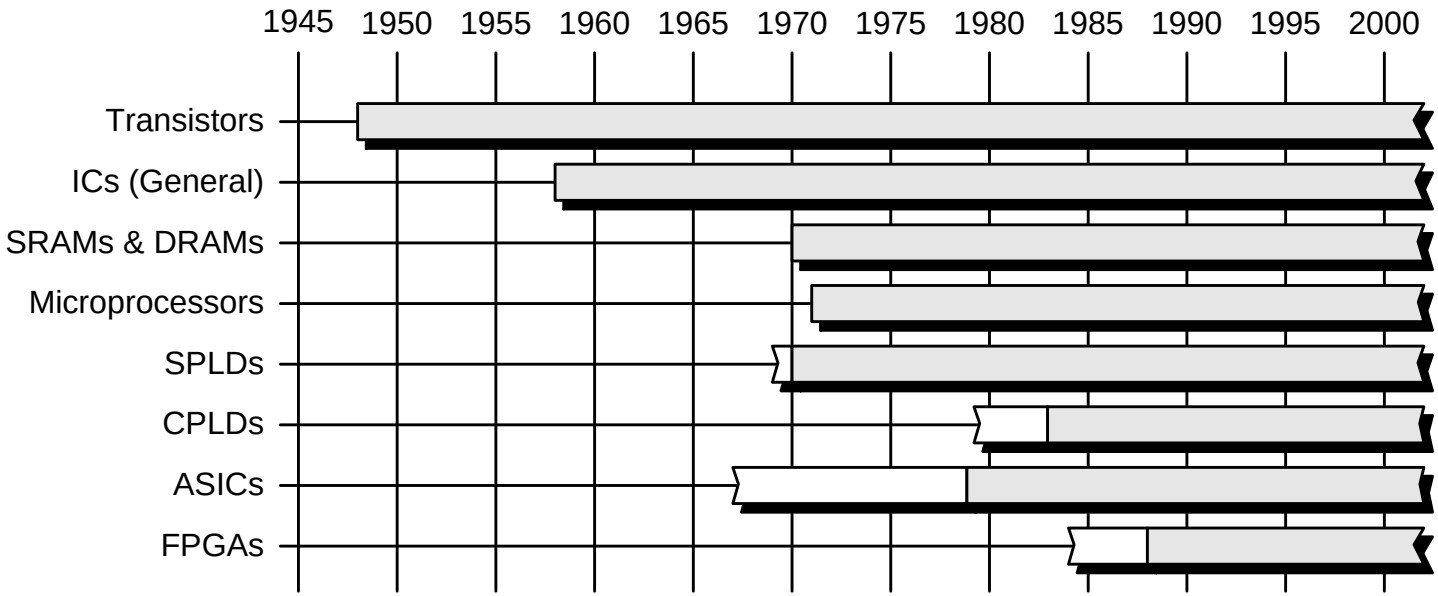
Time line of Programmable devices



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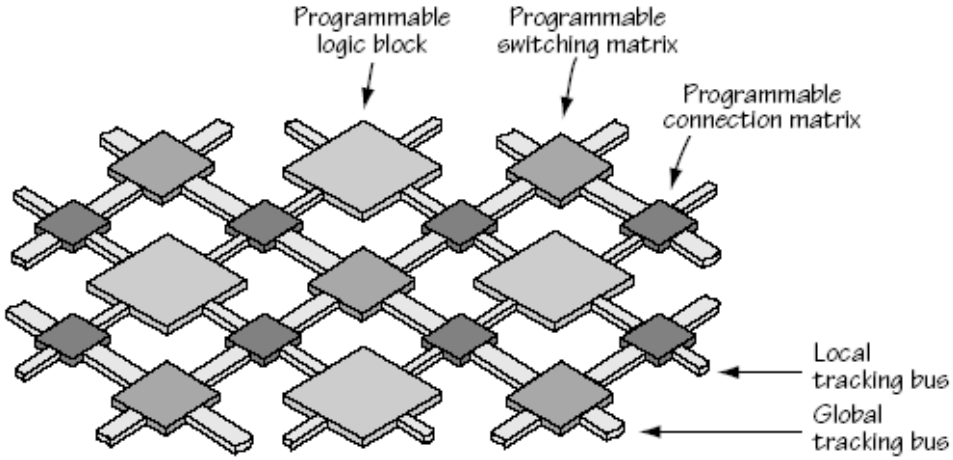
Field Programmable Gate Arrays FPGA

- **Field Programmable Gate Array**
  - **'Simple' Programmable Logic Blocks**
  - **Massive Fabric of Programmable Interconnects**
  - **Standard CMOS Integrated Circuit fabrication process as for memory chips (Moore's Law)**

Huge Number of Logic Block 'Islands'

1,000 … 100,000's +

in a 'Sea' of Interconnects



FPGA Architecture

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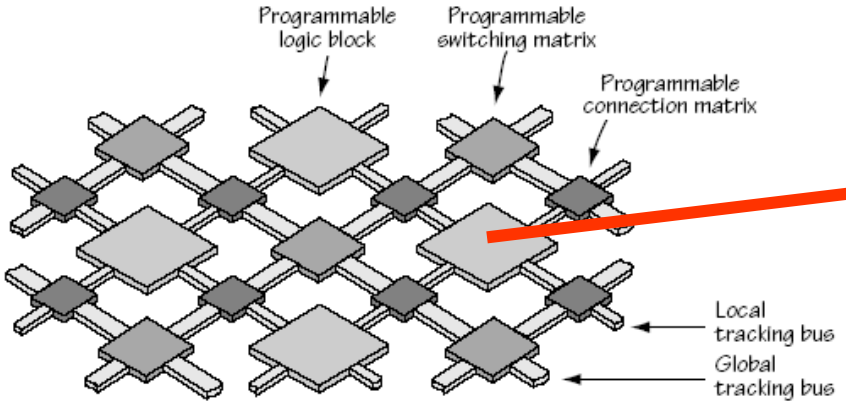
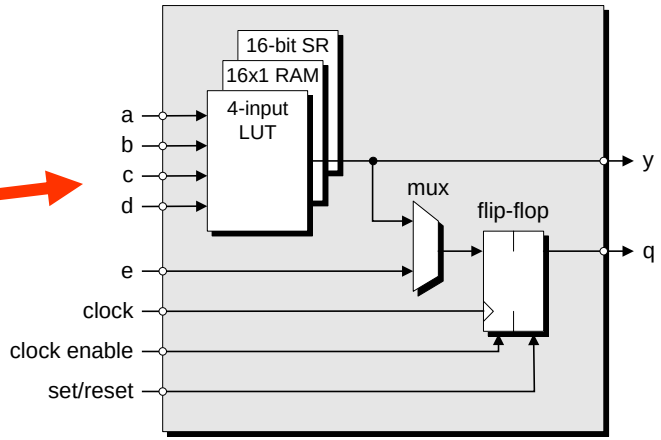
Logic Blocks

- **Logic Functions implemented in Look Up Table LUTs. Truth Tables.**
- **Flip-Flops. Registers. Clocked Storage elements.**
- **Multiplexers (select 1 of N inputs)**



FPGA Fabric



Logic Block

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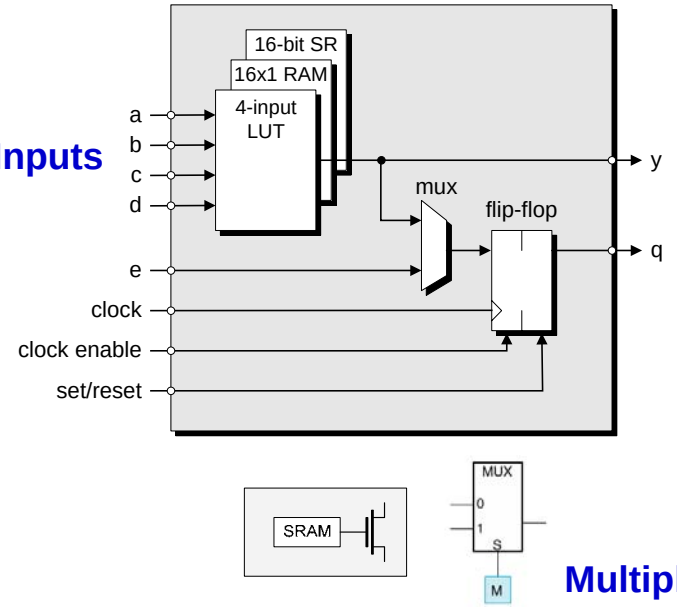
Look Up Tables LUTs

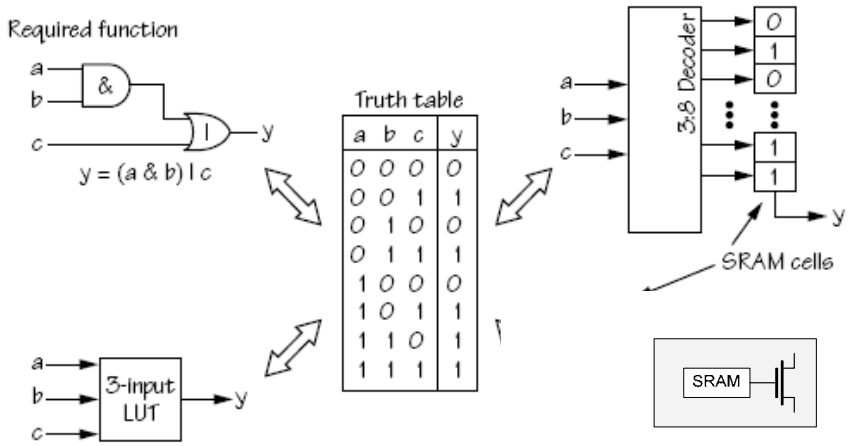
- **LUT contains Memory Cells to implement small logic functions**
- **Each cell holds ‘0’ or ‘1’ .**
- **Programmed with outputs of Truth Table**
- **Inputs select content of one of the cells as output**

3 – 6 Inputs



Multiplexer MUX

3 Inputs LUT -> 8 Memory Cells



Static Random Access Memory SRAM cells

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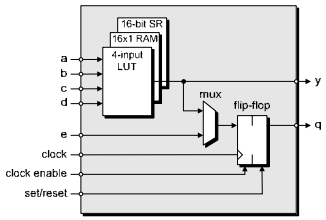
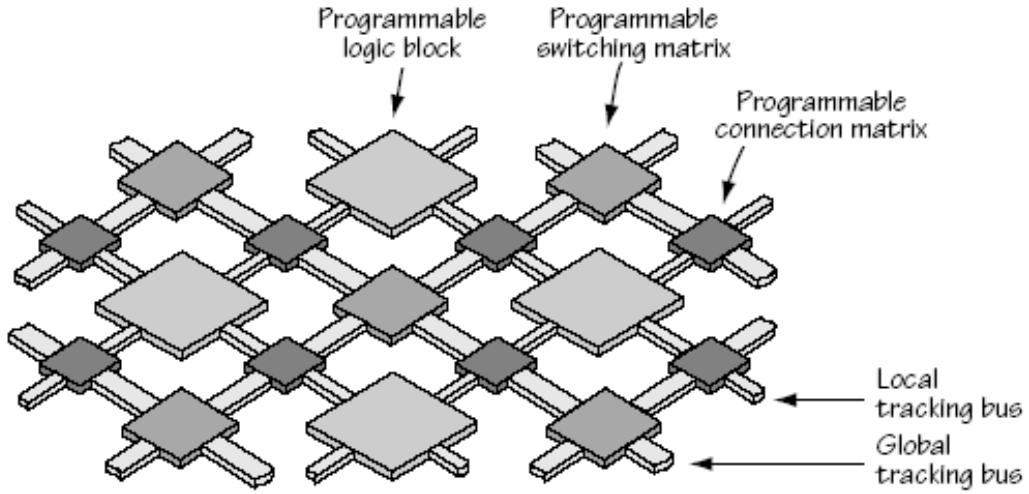
Logic Blocks

- **Larger Logic Functions built up by connecting many Logic Blocks together**





Fabric also has Larger Memory Blocks Block SRAM useful for Data storage

And other "Hard Wired" logic blocks Eg CPUs, Memory Controllers…

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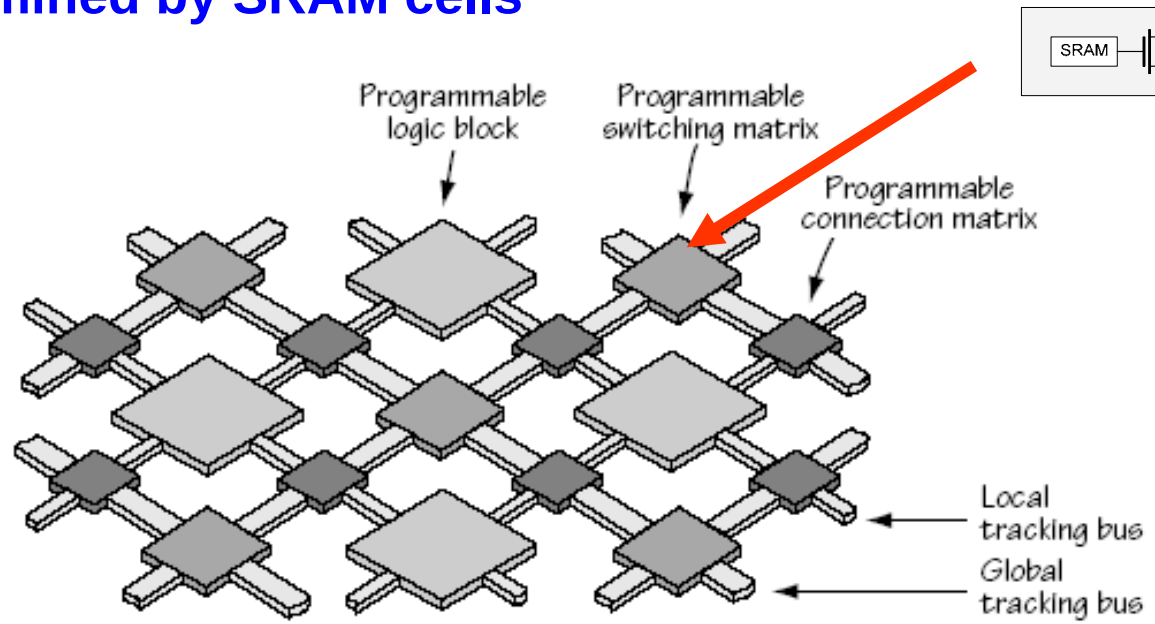
Programmable Routing

- **Connections Routing signals between Logic Blocks**
- **Determined by SRAM cells**



Special Routing for Clocks

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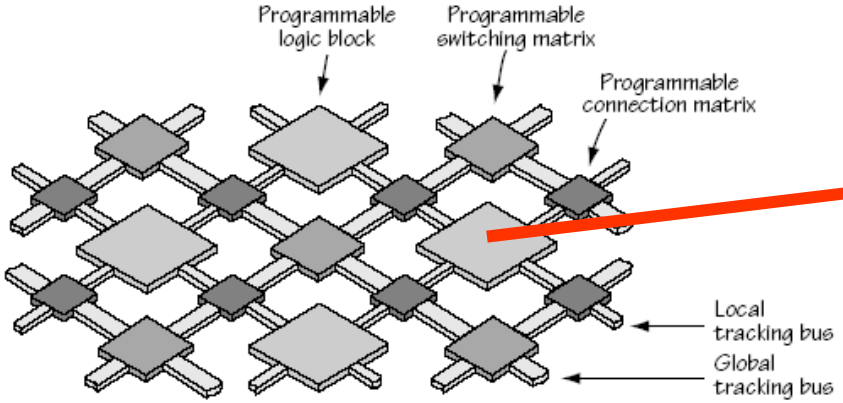
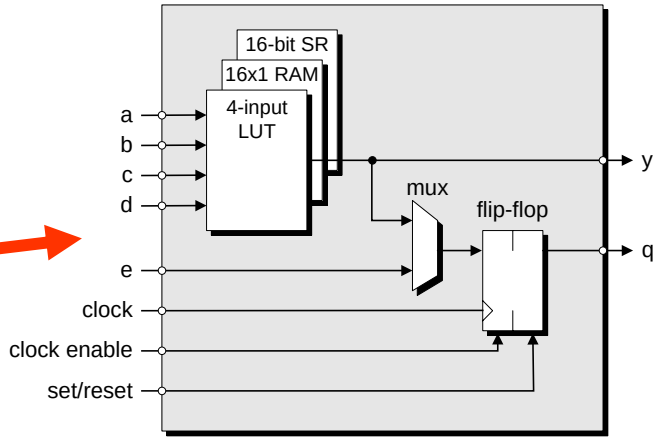
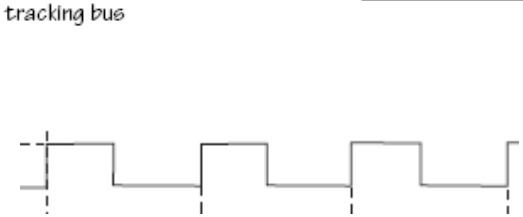
Clocked Logic

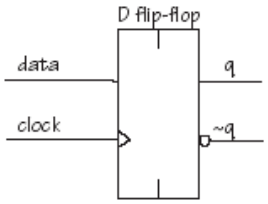
- **Registers on outputs. CLOCKED storage elements.**
- **Sequential Logic Functions (cf Combinational Logic LUTs)**
- **Synchronous FPGA Logic Design, Pipelined Logic.**
- **FPGA Fabric driven by Global Clock (e.g. LHC BX frequency)**



FPGA Fabric







Clock from Outside world (eg LHC bunch frequency)

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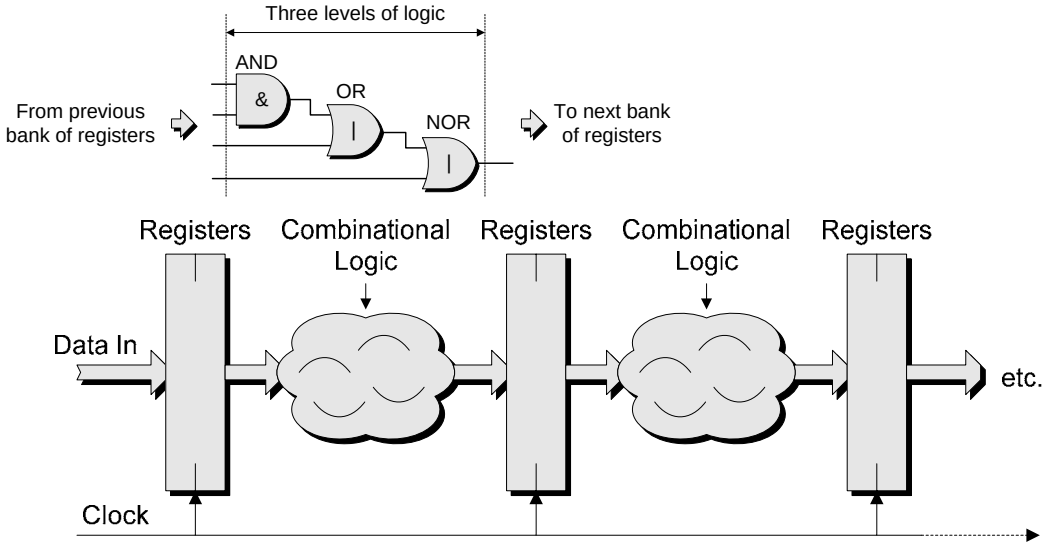
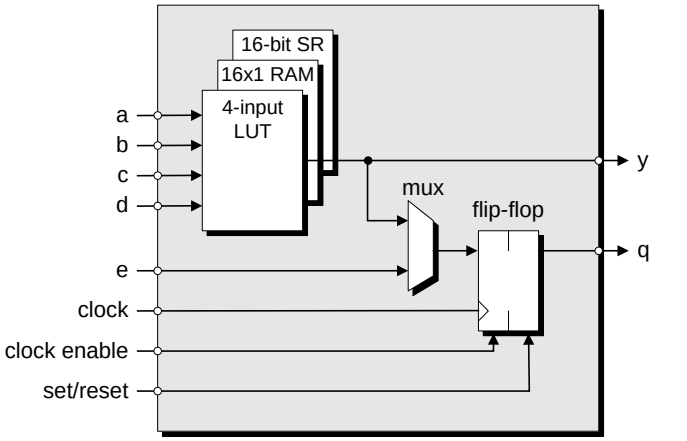
Pipeline

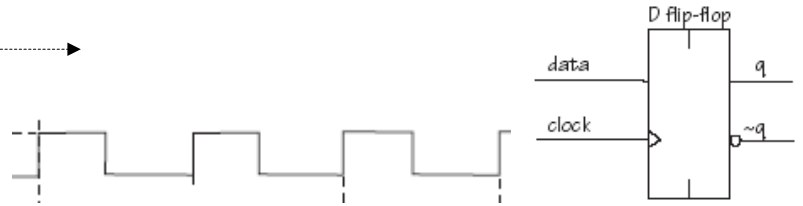
- **Split the task into smaller steps with Registers in between.**
- **All driven by common clock**



Pipeline (Car Assembly Line)

Massively Parallel





Clock

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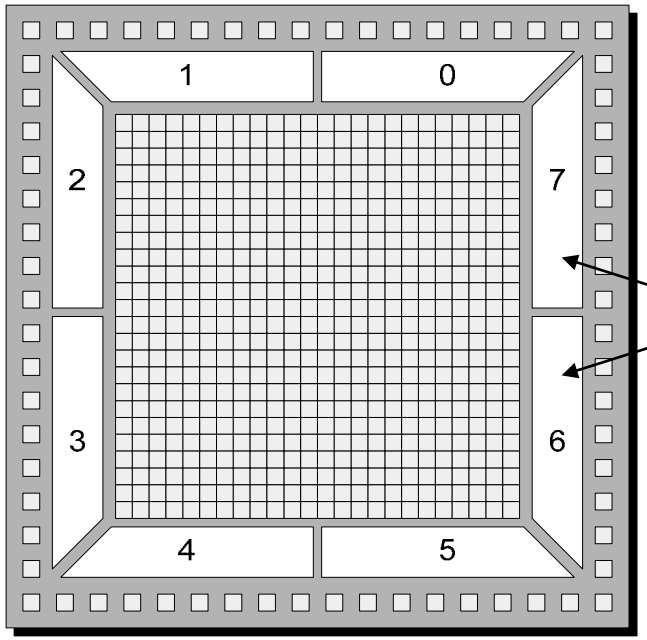
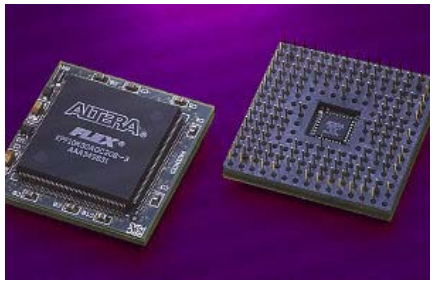
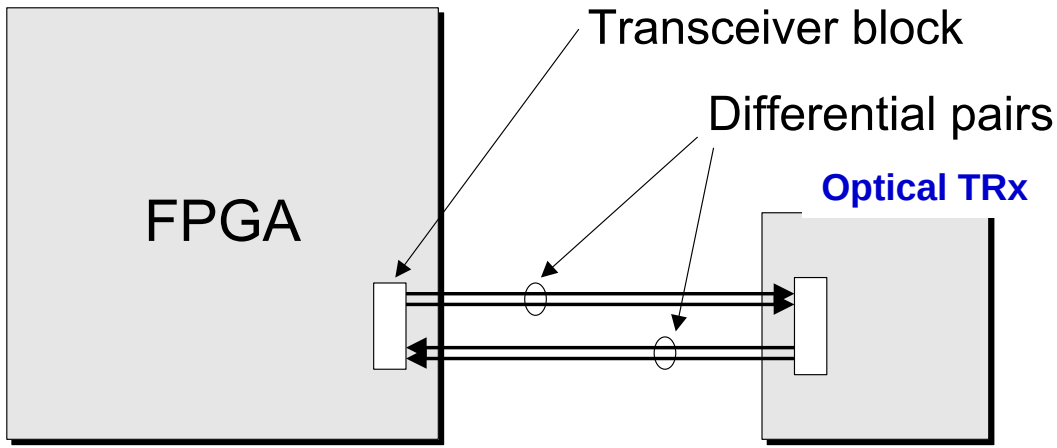
Input Output I/O Getting data in and out





Up to > 1,000 I/O "pins" (several 100 MHz)

Special I/O SERIALISERS
~ 10 GHz transfer rates



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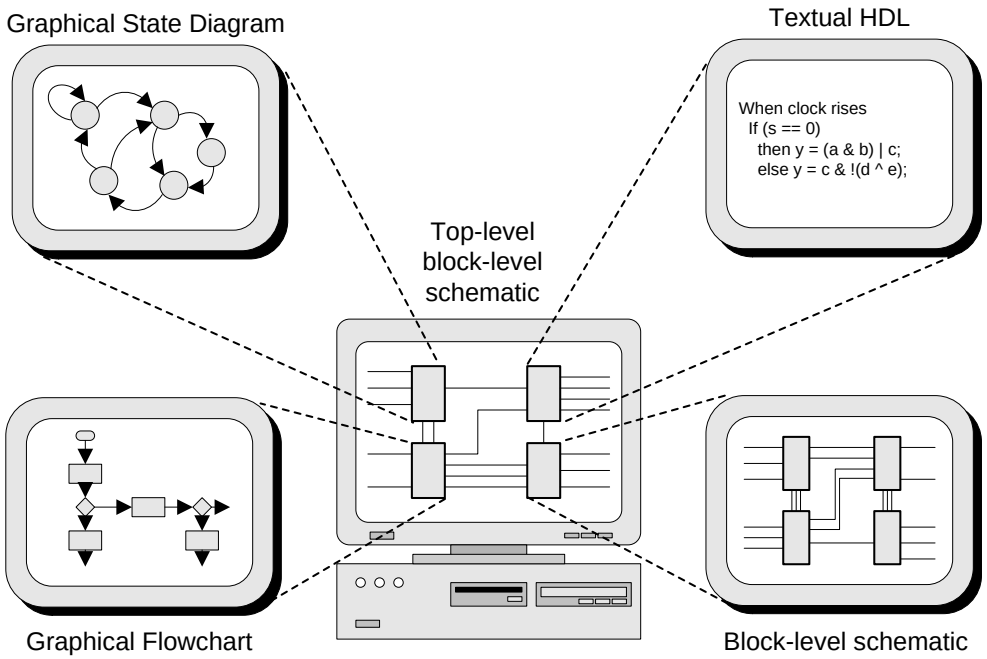
Designing Logic with FPGAs

- **Design Capture.**
- **High level Description of Logic Design.**
  - **Graphical descriptions**
  - **Hardware Description Language (Textual)**



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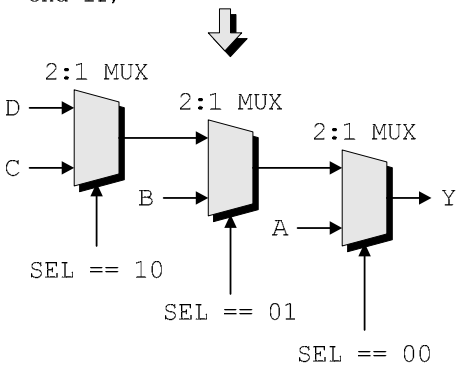
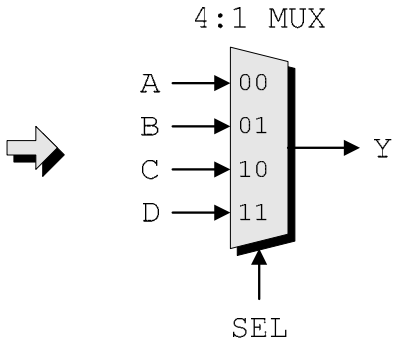
Hardware Description Languages

- Language describing hardware (Engineers call it FIRMWARE)
- Doesn't behave like "normal" programming language 'C/C++'
- Describe Logic as collection of Processes operating in Parallel
- Language Constructs for Multiplexers, FlipFlops …etc
- Compiler (Synthesis) Tools recognise certain code constructs and generate appropriate logic
- Popular languages are VHDL , VERILOG

```
if      SEL == "00" then Y = A;
elseif SEL == "01" then Y = B;
elseif SEL == "10" then Y = C;
else                    Y = D;
end if;
```




```
case SEL of;
     "00": Y = A;
     "01": Y = B;
     "10": Y = C;
otherwise: Y = D;
end case;
```



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The Design Warrior's Guide to FPGAs
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VHDL Firmware

```
architecture Behavioral of dpmbufctrl is
```

Architecture / Logic Module

```
  signal acount       : std_logic_vector(31 downto 0);
  signal dcount       : std_logic_vector(31 downto 0);
  signal bram_addr_i  : std_logic_vector(31 downto 0);

begin

bram_en <='1';
bram_rst <= '0';

--bit order reverse address and data buses to match EDK scheme
bram_addr(0 to 31) <= bram_addr_i(31 downto 0);


--N.B. EDK DOCM addresses are byte orientated count in 4s for whole words

g1 : process(clk, rst)
```

Signals / Input Output to Module

Cf High Level Software Language C, C++

Functions **Parallel Processes**

```
    variable state  : integer range 0 to 3;
                variable buf_zone: integer range 0 to 1;
```

Variables

```
begin
```

Code Blocks

```
              if clk'event and clk = '1' then
                            if rst = '1' then
                                buf_zone:=0;
                                            acount <= (others => '0');
                                            dcount <= (others => '0');
                                            bram_wen <= (others => '0');
                                            bram_addr_i <= X"00001FFC"; --
                                            bram_dout_i <= (others => '0');
                                            state:=0;
                                elsif state = 0 then
                                            --wait for din(0) at address 1FFC to be set to zero
                                            --what about pipeline of BRAM - need to wait before polling?
                                            bram_wen <= (others => '0');
                                            acount <= (others => '0');
                                            bram_addr_i  <= X"00001FFC";
                                            bram_dout_i <= (others => '0');
                                            dcount <= dcount;
                                            if bram_din_i = X"00000000
                                                        state := 1;
                                            else
                                                        state := 0;
                                            end if;
```

Clocked Logic / Registers

Signal Assignments

If Else Blocks **Multiplexers**

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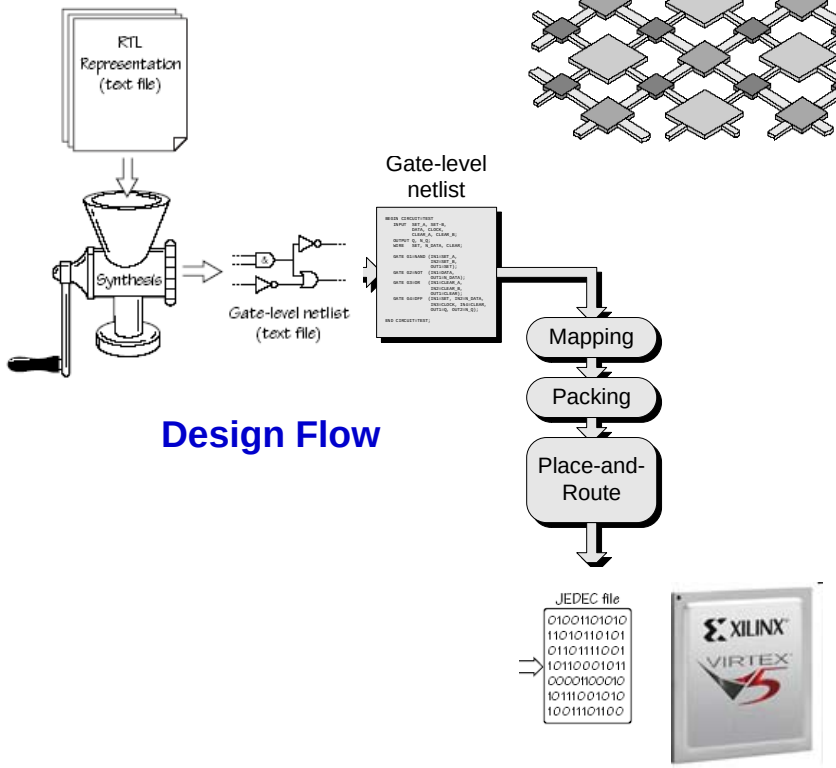
Designing Logic with FPGAs

- **High level Description of Logic Design**
  - **Graphical descriptions**
  - **Hardware Description Language (Textual)**
- **Compile (Synthesis) into NETLIST.**
- **Boolean Logic Gates.**
- **Target FPGA Device**
  - **Mapping**
  - **Routing**
- **Bit File for FPGA**
- **Commercial CAE Tools (Complex & Expensive)**
- **Logic Simulation**



Design Flow

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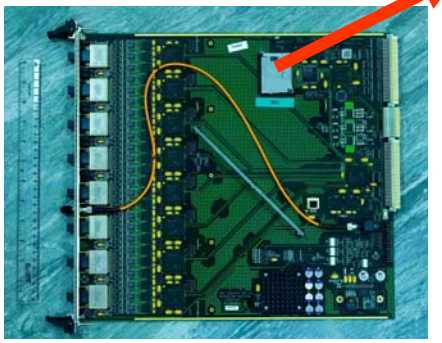
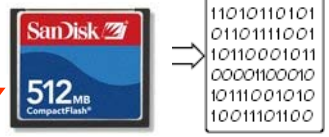
Configuring an FPGA

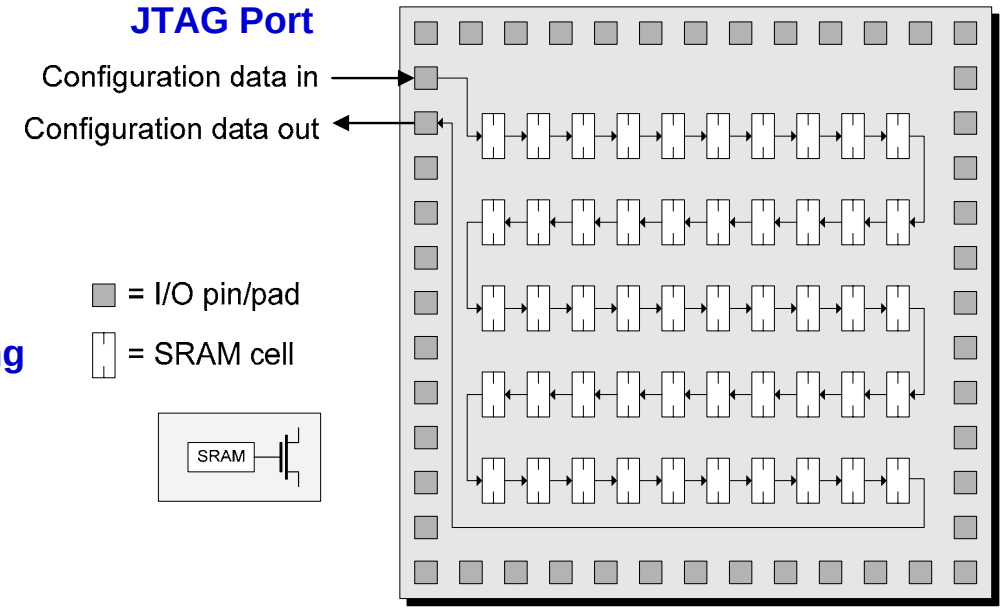
- **Millions of SRAM cells holding LUTs and Interconnect Routing**
- **Volatile Memory. Lose configuration when board power is turned off.**
- **Keep Bit Pattern describing the SRAM cells in non-Volatile Memory e.g. PROM or Digital Camera card**
- **Configuration takes ~ secs**





Programming Bit File

JTAG Testing



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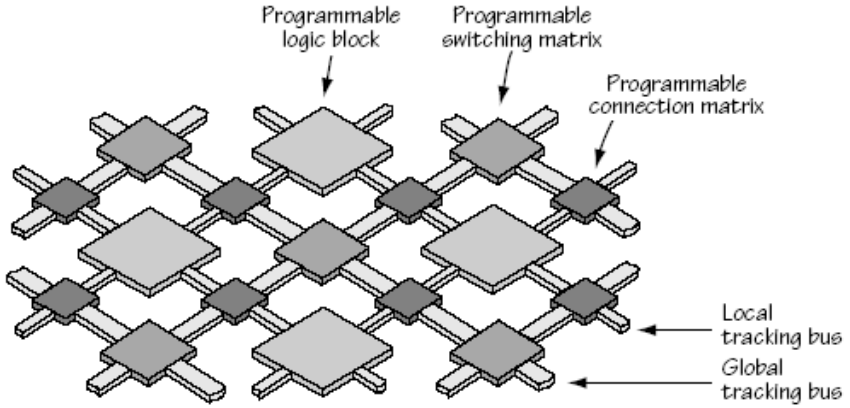
Field Programmable Gate Arrays FPGA

- **Large Complex Functions**
- **Re-Programmability, Flexibility.**

- **Massively Parallel Architecture**
- **Processing many channels simultaneously cf MicroProcessor sequential processing**

- **Fast Turnaround Designs ☺**
- **Standard IC Manufacturing Processes ☺**
- **Leading Edge of Moore's Law ☺**
- **Mass produced. Inexpensive. ☺**
- **Many variants. Sizes. Features. ☺**

- **Not Radiation Hard ☹**
- **Power Hungry ☹**



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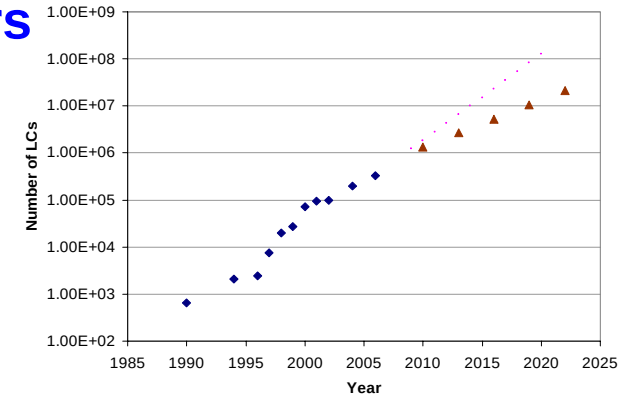
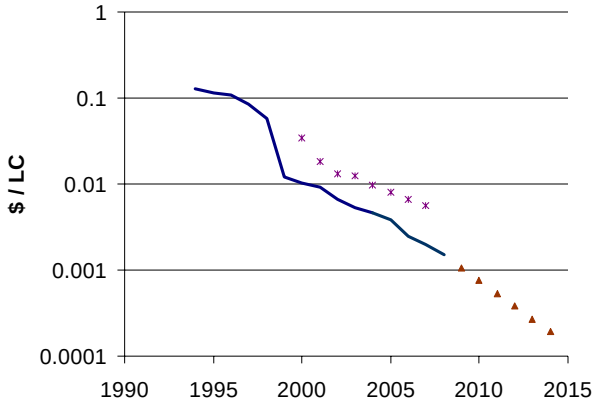
FPGA Trends

- State of Art is 40nm on 300 mm wafers
- Top of range >100,000 Logic Blocks
- >1,000 pins (Fine Pitched BGA)



- Logic Block cost ~ 1$ in 1990



- Problems
  - Power. Leakage currents.
  - Design Gap
    - CAE Tools

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Summary

- **Programmable Logic Devices**
  - **Basics**
  - **Evolution**

- **FPGA Field Programmable Gate Arrays**
  - **Architecture**

- **Design Flow**
  - **Hardware Description Languages**
  - **Design Tools**

Importance for Particle Physics Experiments

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