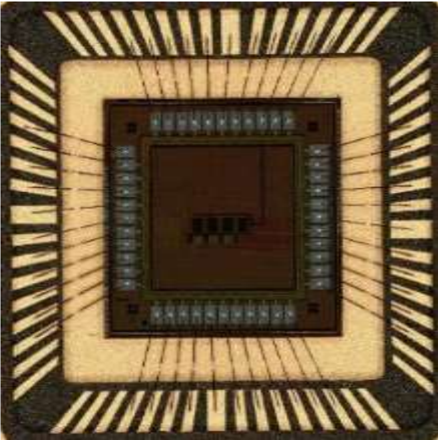
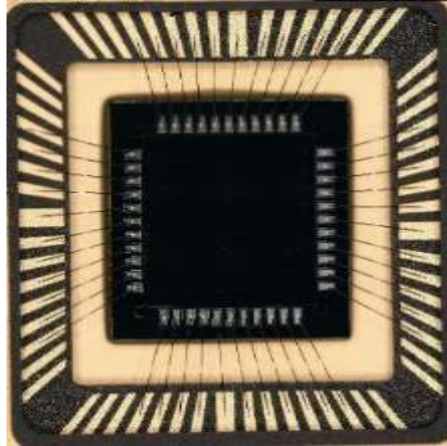




The Open University

Design and Performance of a Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias

13 September 2017

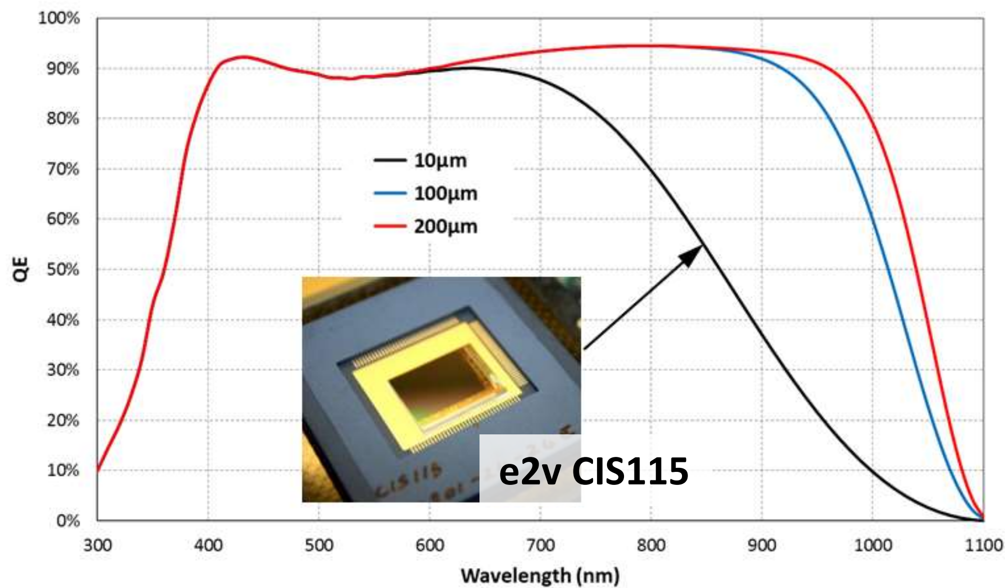
Konstantin Stefanov

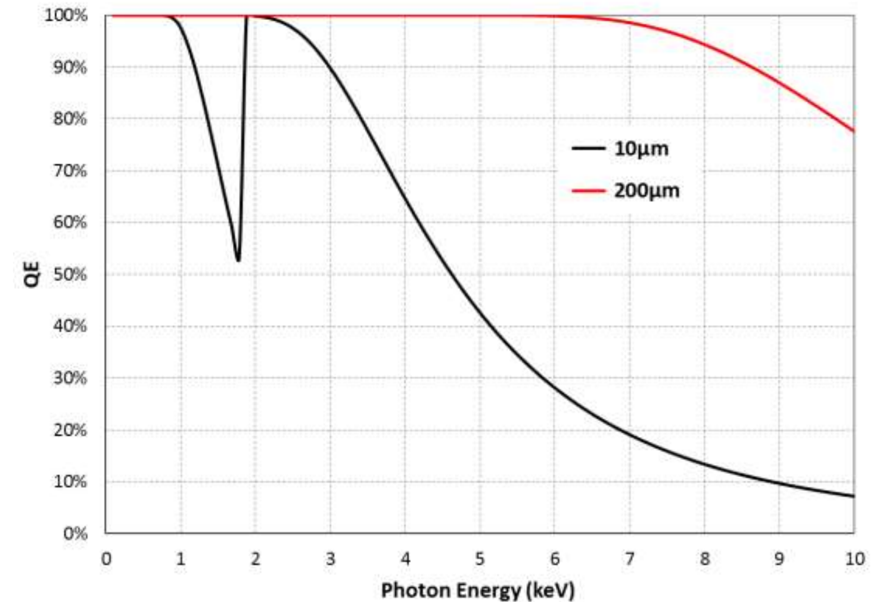
Contents

- **Background**
- **Goals and objectives**
- **Overview of the work carried out during this project:**
  - **Chip design and layout**
  - **TCAD simulations**
  - **Chip characterisation**
  - **Papers and publicity**
- **Summary**

Background

- Demand for thick (>100 µm), fully depleted CMOS sensors for high QE
- Near-IR imaging : astronomy, Earth observation, hyperspectral imaging, high speed imaging, spectroscopy, microscopy and surveillance.
- Soft X-ray (<10 keV) imaging at synchrotron light sources and XFELs (substrate thickness >200 µm)

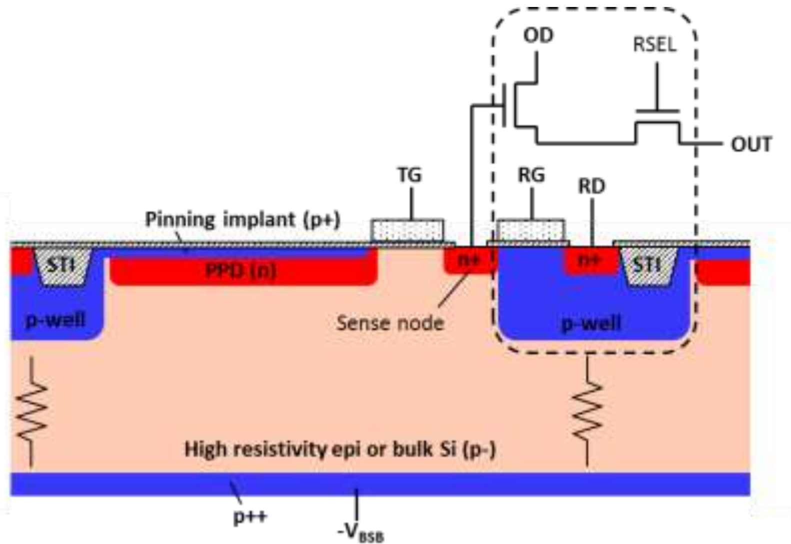


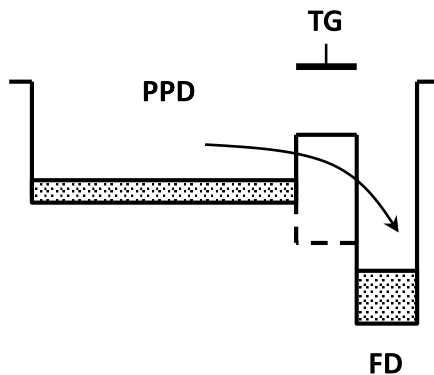


Goals and Objectives

- Main goal:
  - Develop the technology for achieving large depleted depths in pinned photodiode CMOS image sensors, leading to high QE in near-IR and soft X-rays
  - Make the technology available commercially through Teledyne e2v
- Objectives for this work:
  - Simulate and design a prototype, proof of principle sensor
  - Manufacture the chip using a commercial foundry
  - Characterise the devices
  - Publish papers and disseminate the results
- Funded by UKSA

The Pinned Photodiode Pixel (PPD, 4T)

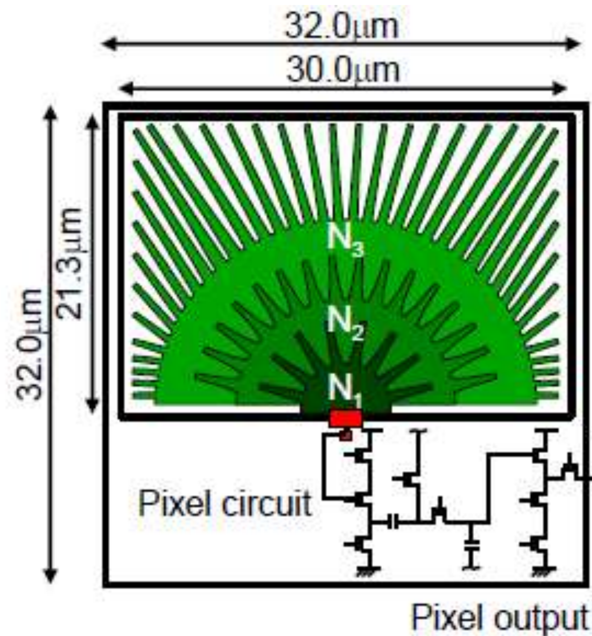


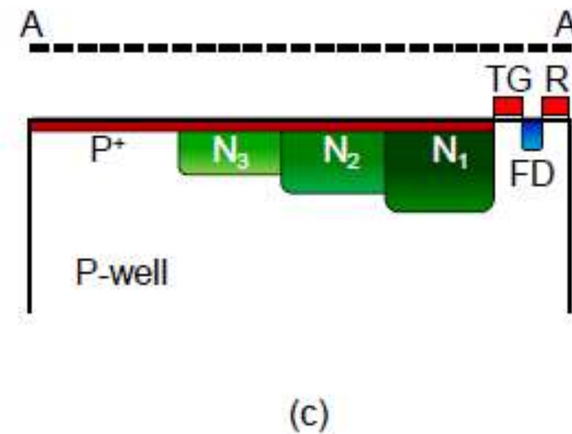


- PPD is the preferred CMOS imaging element now
- Charge is collected in a potential well and then transferred to the sense node (FD)
- Widely used, excellent performance
  - Noise could be <1 e- RMS
  - Correlated double sampling comes naturally
  - Small sense node, high responsivity
  - Very low dark current
- However:
  - The peak voltage in the PPD (V_{pin}) is low ≈1.5V
  - Charge transfer is slow (tens or hundreds of ns), large pixels can have image lag
  - Reverse biasing is the only way to deplete thick material, but is problematic

Accelerated charge transport in PPD

K. Miyauchi et al., Proc. of SPIE-IS&T/ Vol. 9022 902203-1





- **Increased diode doping concentration towards the sense node (FD)**
- **Higher doping causes higher potential**
- **Creates potential gradient towards the sense node**
  - **Electric field is small (500 V/cm), but enough to make a difference**

Performance

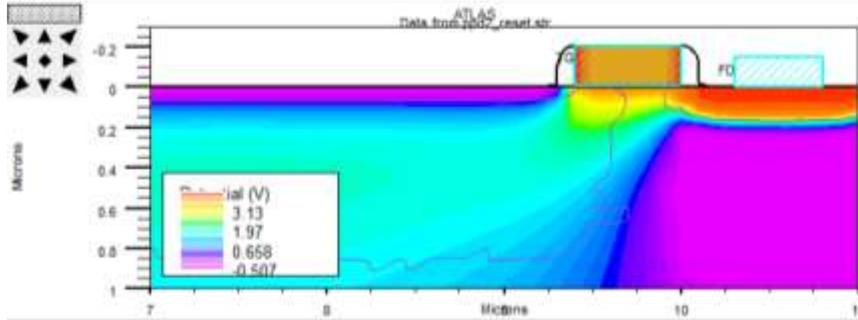
- **Charge collection of 96% in 10 ns due to the large depleted diode**
- **Charge transfer within PPD below 10 ns**
- **32 μm pixel used for high speed imaging**
- **20M frames per second achieved in burst mode**
- **Similar approach is used to speed up larger pixels (>100 μm)**

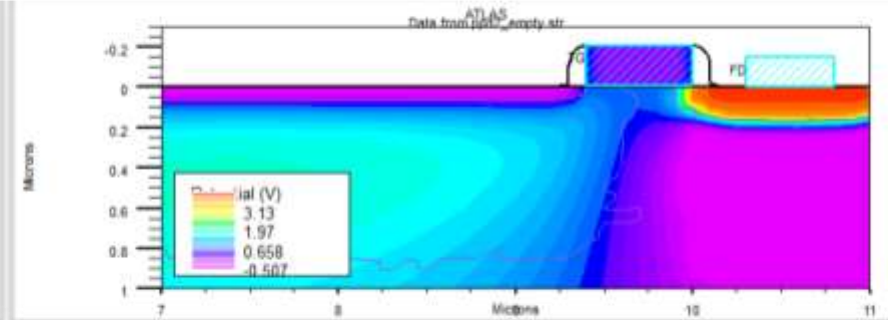
SNR and power dissipation

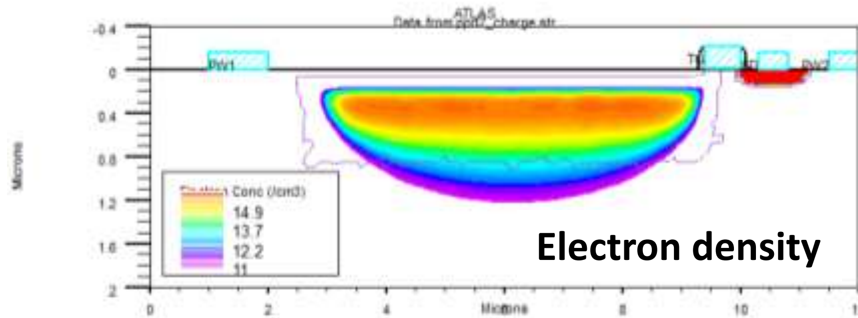
- PPD is ideal for low-power, high SNR detectors
  - Separates the functions of charge collection and charge-to-voltage conversion
  - The PPD can be large, helps with prompt charge collection
  - The node capacitance can be very small – large voltage change
  - MIP signal charge is nearly proportional to detector thickness
- In general :
  - SNR $\sim(Q/C)\sqrt{g_m}$
  - For constant SNR, the power dissipation is $\sim(C/Q)^m$ $(2 \le m \le 4)$*
  - 40 nW/pixel, 2fF node capacitance in ALPIDE (ALICE ITS) achieved
- Very small capacitance would produce a “digital” signal from a MIP, >300 mV needed
  - This would eliminate analogue power!
  - Sensors with conversion gain >100 µV/e- exist now (160 mV from 20 µm Si)

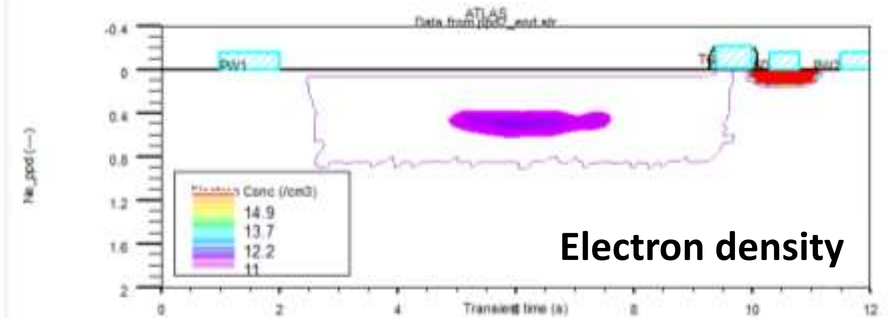
*See the papers from Walter Snoeys in NIMA from 2013 and 2014

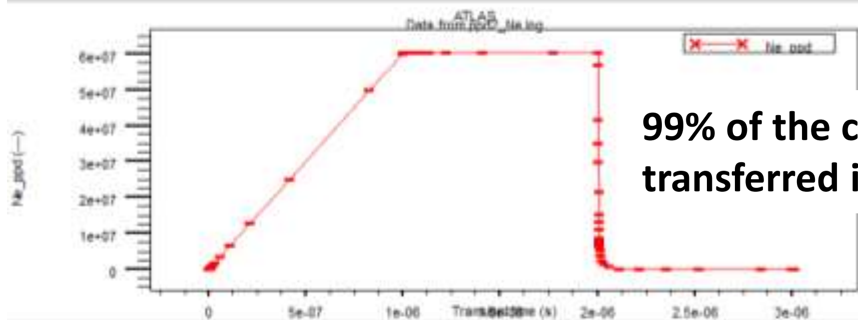
Simulated PPD operation

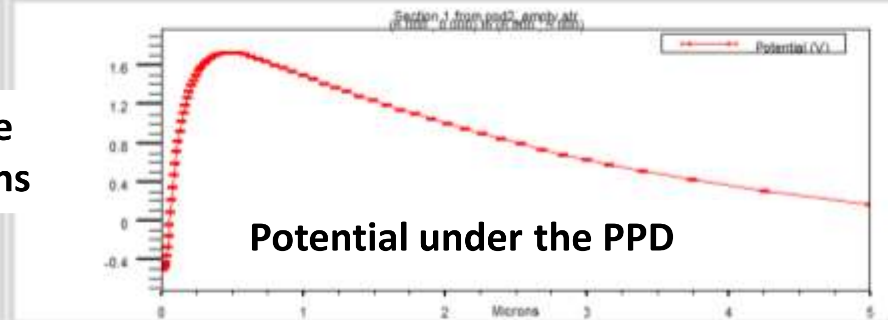












Tonyplot 3.8.46.R © Silva

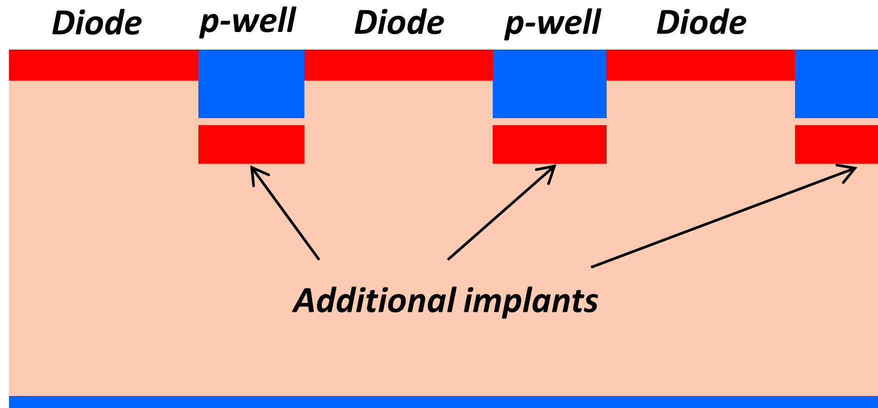
Reverse biasing PPD pixels

P-wells
+Bias
+Bias
+Bias
Diode
Pinch-off
P-type epi/bulk Si
Backside p+ implant
$-V_{reverse}$

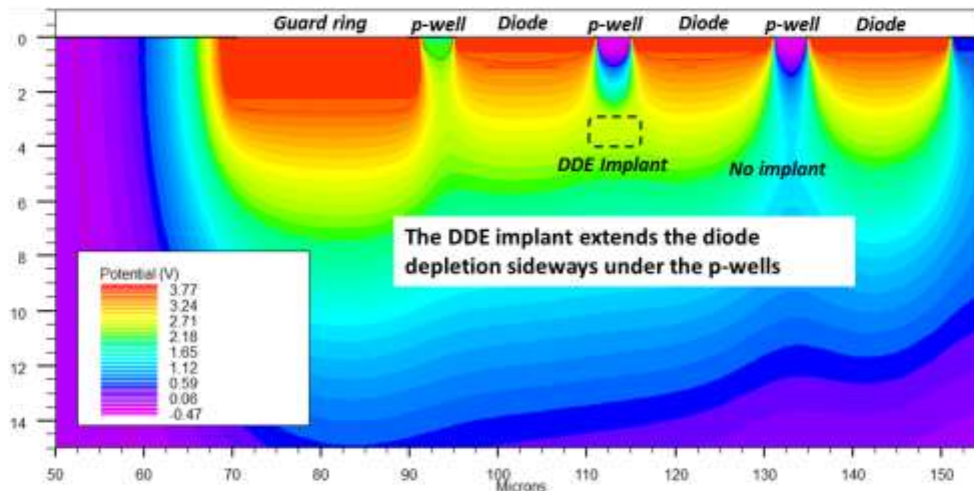
$+V_{PPD}$
$+V_{PPD}$
Diode
Diode
p-well
p-well
p-well
p-type silicon
(a)
Shallow backside p++ implant
V_{BSB}

- If reverse bias $V_{reverse}$ is applied:
  - p+/p/p+ resistor is formed, leakage current flows
  - This has to be eliminated for a practical device
- Pinch-off under the p-wells is needed at all times (merged depletion regions) to prevent leakage
- The pinch-off condition depends on:
  - Doping and junction depth
  - Photodiode and p-well sizes
  - Bias voltages
  - Stored signal charge

Substrate current suppression

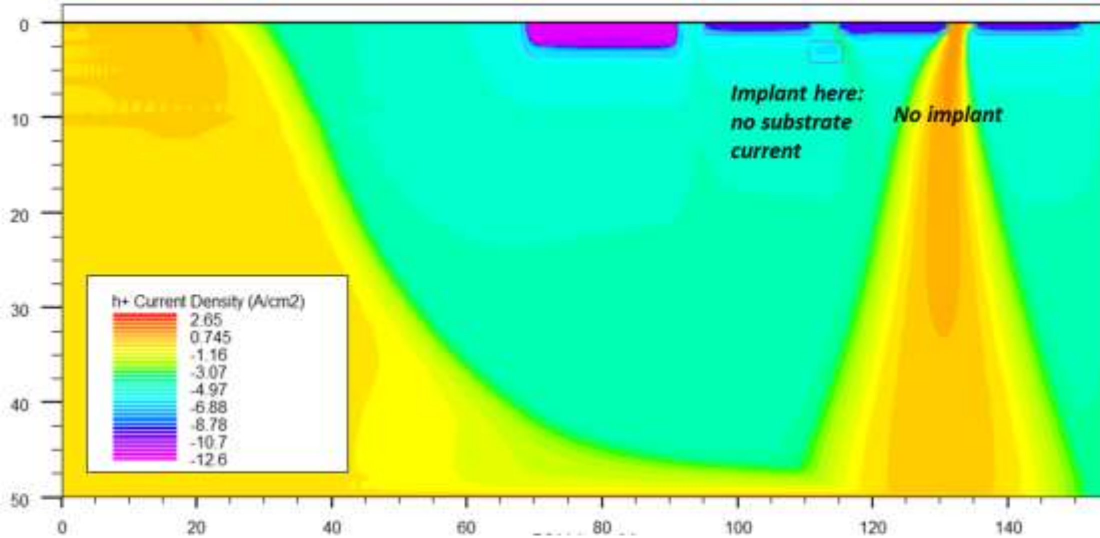


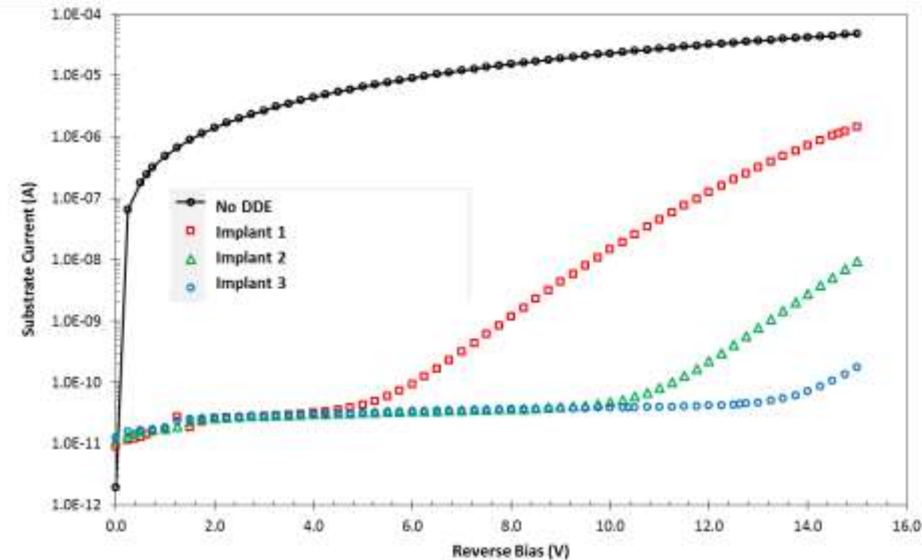
Simplified PPD pixel structure with DDE



- **If the p-wells are deep (as they are usually), pinch-off may not occur**
- **The p-well should be made to be as narrow as possible, but this is not sufficient**
- **Additional n-type implant added:**
  - **Under the p-wells**
  - **Floating**
  - **Called Deep Depletion Extension (DDE)**
- **Patent pending (owned by Teledyne e2v)**

Substrate current





$$I_{BSB} = I_0 + AT^2 S \frac{m_h^*}{m_0} exp\left(-\frac{V_{PW} + \beta V_{BSB}}{kT/q}\right)$$

- **Not a traditional reverse biased diode**
- **Different leakage mechanism**
  - **Thermionic emission of holes over a potential barrier**
  - **Not a “normal” breakdown**
  - **Eventually leakage occurs, however it should be well above full depletion**

Realistic potential profiles @ -5V bias (1)

Realistic potential profiles @ -5V bias (2)

0
1
2
Potential (V)

Potential Y=1.8µm

Potential (V)

1.5
1.0
0.5
0.0

0
5
10
15
20
25
30

X (µm)

Realistic potential profiles @ -5V bias (3)

Potential (V)
3.2
2.67

Potential R-L

Potential (V): 2.0, 1.5, 1.0, 0.5, 0.0, -0.5, -1.0

Distance (µm): 0, 2, 4, 6, 8, 10, 12, 14

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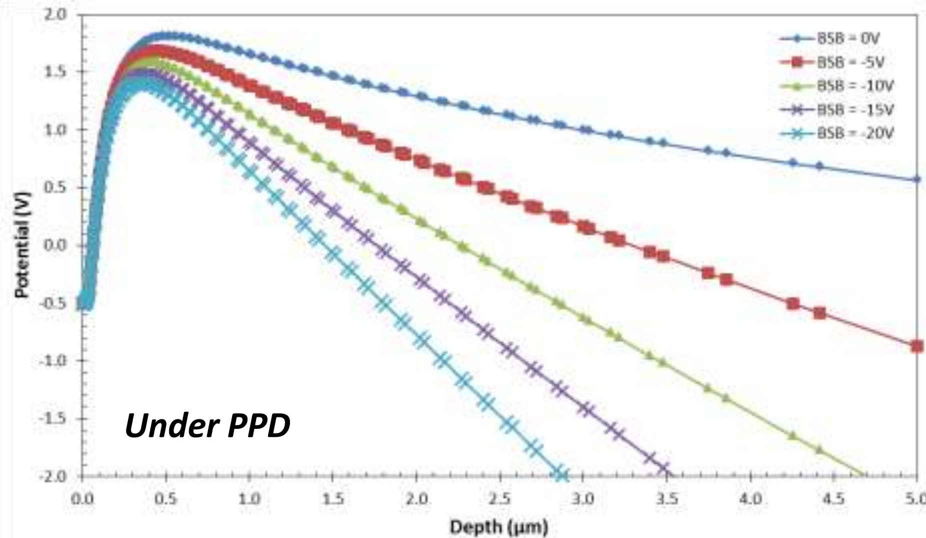
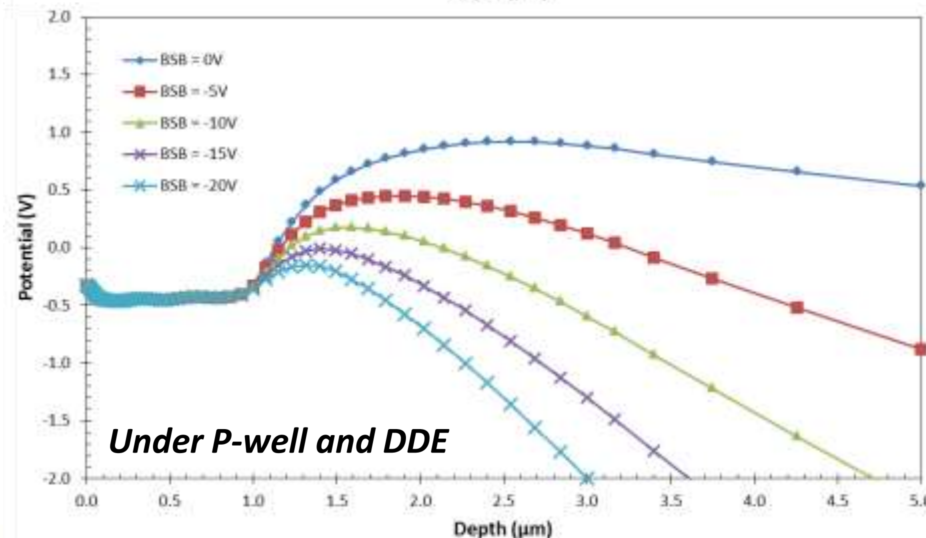
TELEDYNE e2V
Everywhereyoulook™

Konstantin Stefanov, 13 September 2017

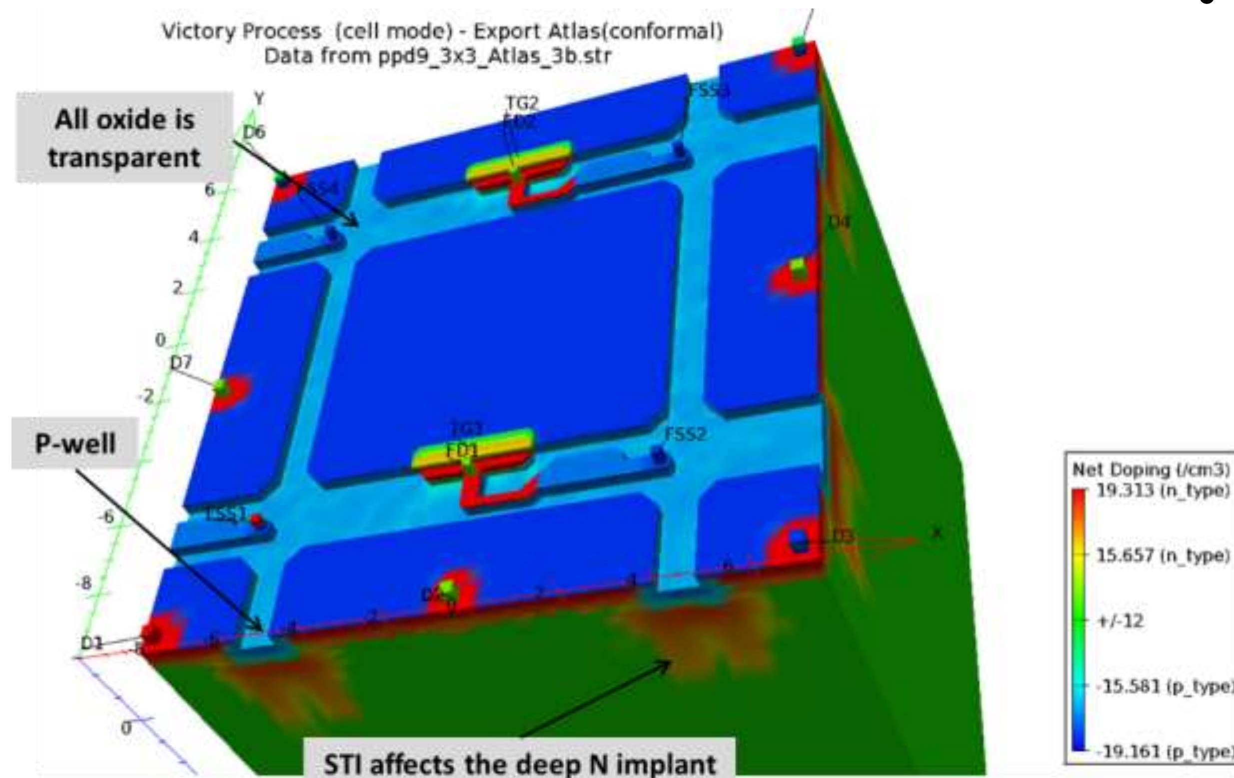
Potentials under the PPD and the P-wells





- As the backside bias increases:
  - The pinning voltage decreases (and the full well capacity too)
  - Front-to-back hole leakage current increases due to thermal excitation over the reduced potential barrier
- DDE implant is optimised:
  - Low doping – doesn't achieve pinch-off
  - High doping – creates a potential pocket

Pixel simulations



- **3D models made and simulated**
  - **Very time consuming, but worth it**
  - **This gave more confidence to proceed with manufacture**

Reverse currents simulated for all 24 different pixel variants:

- **3 implant profiles**
- **Four 10 µm pixel designs**
- **Four 5.4 µm pixel designs**

Substrate current – implant energy dependence

Vpin ≈ 1.7 V

No DDE
Shallow DDE
Middle DDE
Deep DDE

Substrate Current (A)

1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12

0.0 2.0 4.0 6.0 8.0 10.0 12.0 14.0 16.0

Reverse Bias (V)

Substrate current – implant size dependence

Vpin ≈ 1.7 V

Substrate Current (A)

1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12

Baseline
Size 1
Size 2 > Size 1
Size 3 > Size 2

0.0 2.0 4.0 6.0 8.0 10.0 12.0 14.0 16.0

Reverse Bias (V)

Potential pockets in depth, 0.5 µm steps

Deep DDE

ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14

ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14_1.str

ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14_2.str

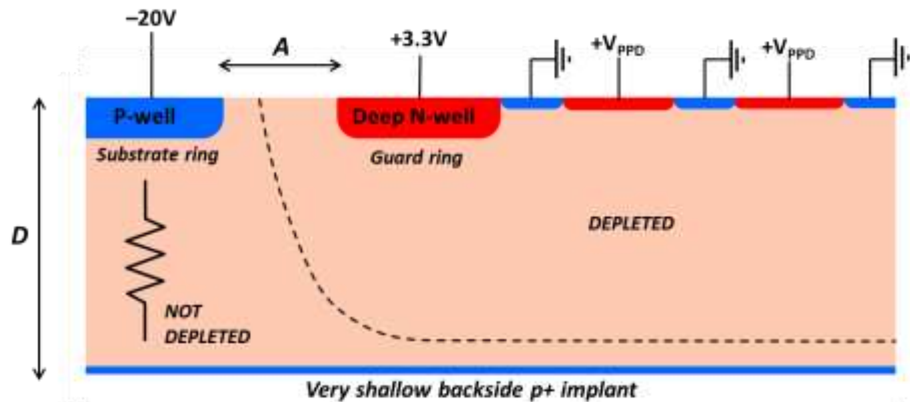
ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14_3.str

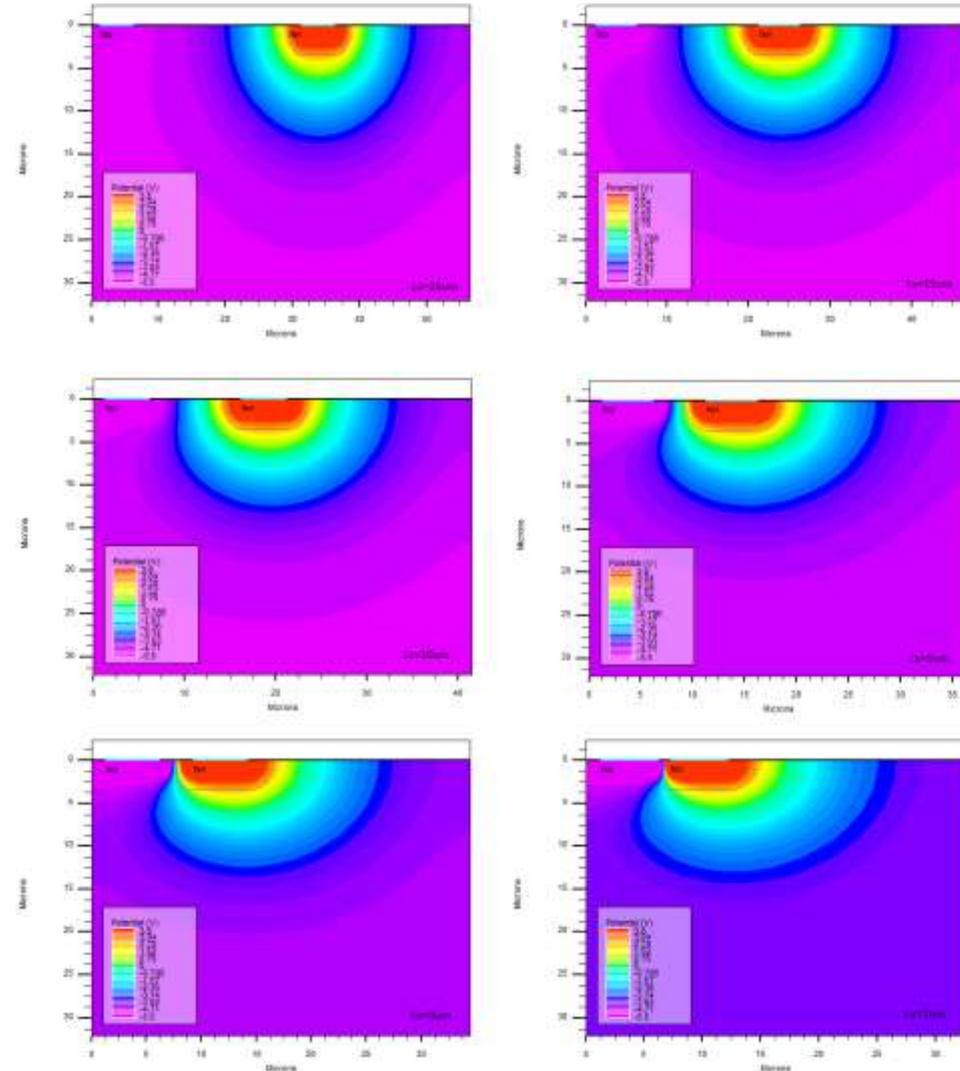
ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14_4.str

ATLAS
Data from ppd9_3x3_bss_5V_1d_slice_14_5.str

Pockets

Backside biasing

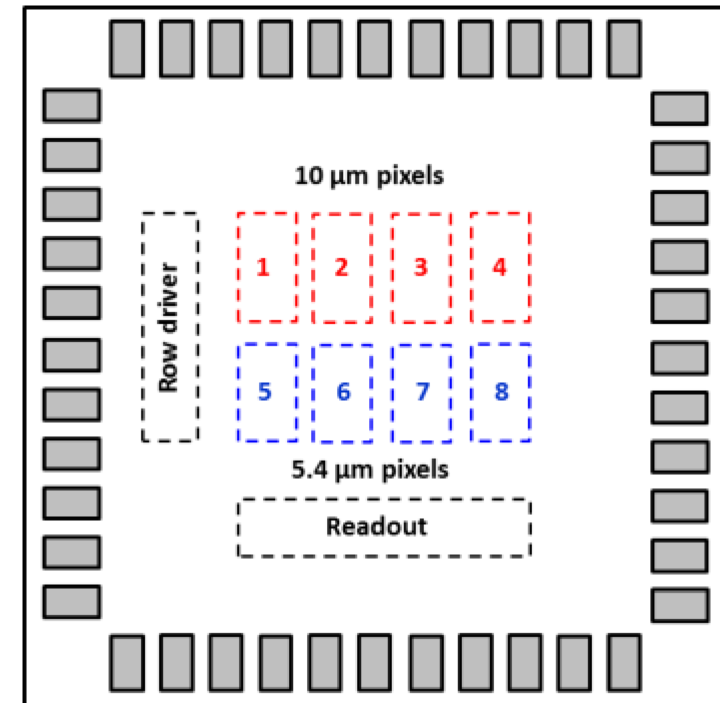




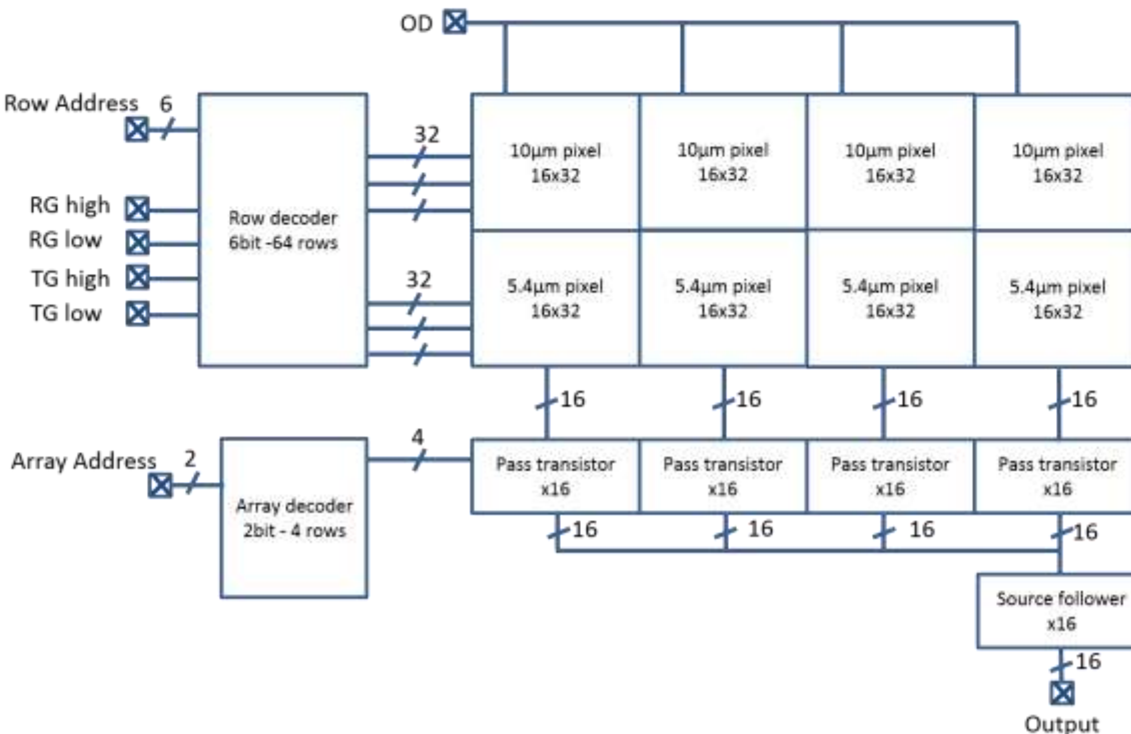
- Distance *A* should be big enough to prevent electric breakdown
  - 10 µm is OK up to -50V, from experimental data
- The depletion can undercut the conductive path from the front side P-well to the back side
  - In our design the substrate p-well is 600 µm wide : not an issue

Chip design

- Made on 18 µm 1 kΩ.cm epi, as a proof of principle
  - This method applies to any thickness
- Based on a PPD provided by TowerJazz, modified by the CEI
- Prototyping 10 µm and 5.4 µm pixel designs, two V_{pin} (low=1.5V and high=1.7V)
  - 8 pixel arrays of 32 (V) × 20 (H) pixels each
- Each array explores different shape and size of the DDE implant
  - One reference design without DDE (plain PPD pixel)
- Custom ESD protection designed



Chip design



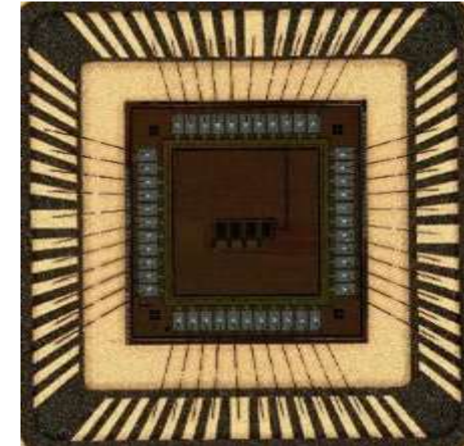
- Design kept as simple as possible
- Only the bare minimum of electronics:
  - Row address decoder selects a row from 0..63
  - Array decoder selects which array to be read out: 0..3
- Each electrical array has 32 rows of 10 µm pixels and 32 rows of 5.4 µm pixels

Whole sensor cross section

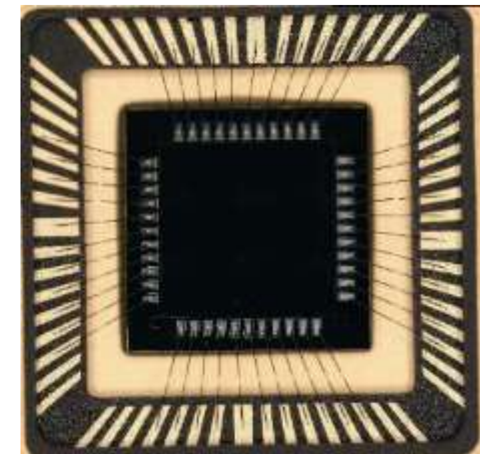
- Main difference with the typical PPD CIS – all area outside the pixels is N-type implanted (N-well and deep N-well) and reverse biased
- All non-pixel circuitry is on top of deep N-well
- The exception is the backside bias region

Chip manufacture

- Submitted for manufacture on 22 February 2016
- 18 custom-processed wafers delivered in July 2016
  - 60 chips diced by TowerJazz
  - 12 intact wafers for back-thinning
- 18 front side illuminated (FSI) chips wire-bonded
- Two wafers back-thinned at Teledyne e2v
  - 10 backside illuminated (BSI) chips wire-bonded
- All 28 chips worked without defects (100% yield)



FSI



BSI

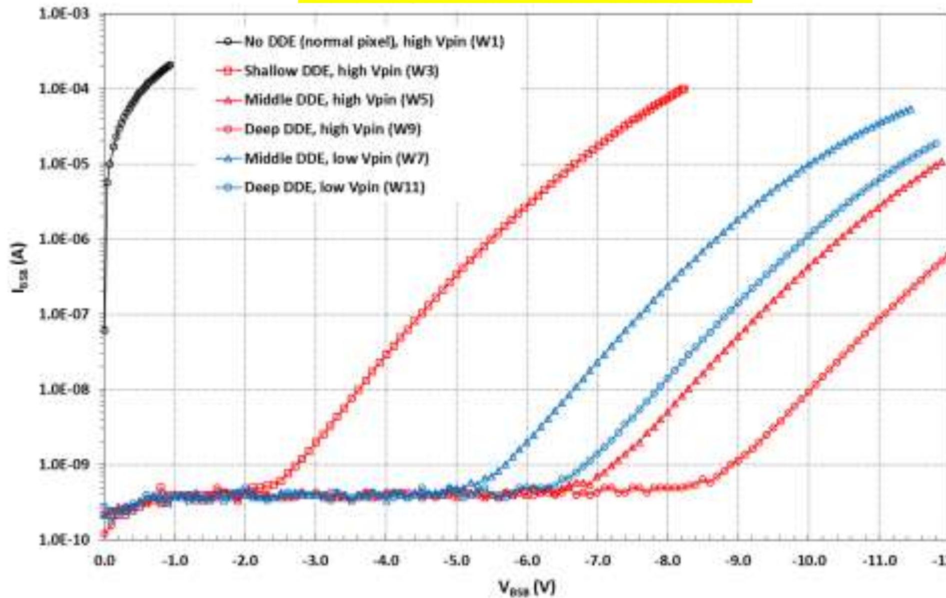
DDE implant	Low Vpin (1.5-1.6V)	High Vpin (1.7-1.8V)
None	---	Wafers 1, 2, 13
Shallow	---	Wafers 3, 4, 14
Medium	Wafers 7, 8, 16	Wafers 5, 6, 15
Deep	Wafers 11, 12, 18	Wafers 9, 10, 17

Experimental setup

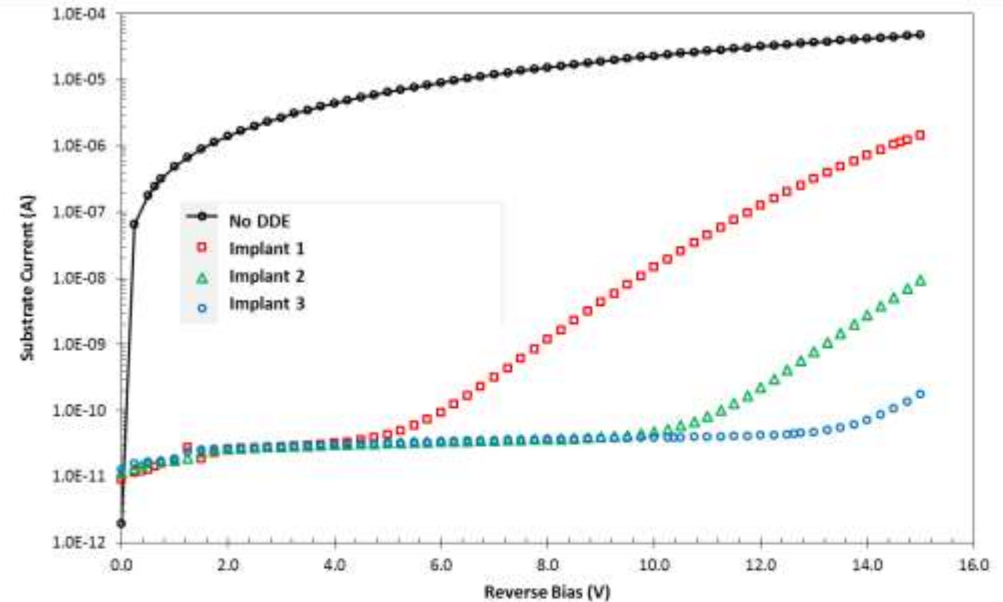
- A test board designed and assembled at the CEI for the FSI chip variants
- Controlled by LabVIEW with National Instruments FPGA card
  - 8 ADC, 8 DAC, 16 digital I/O signals
  - Works at 500 kpix/s readout, 16-bit data
- Adapter board from FSI to BSI chips
- A 3-channel source measure unit used for the I-V characteristics
  - 100 pA resolution

Reverse biasing

Measurement

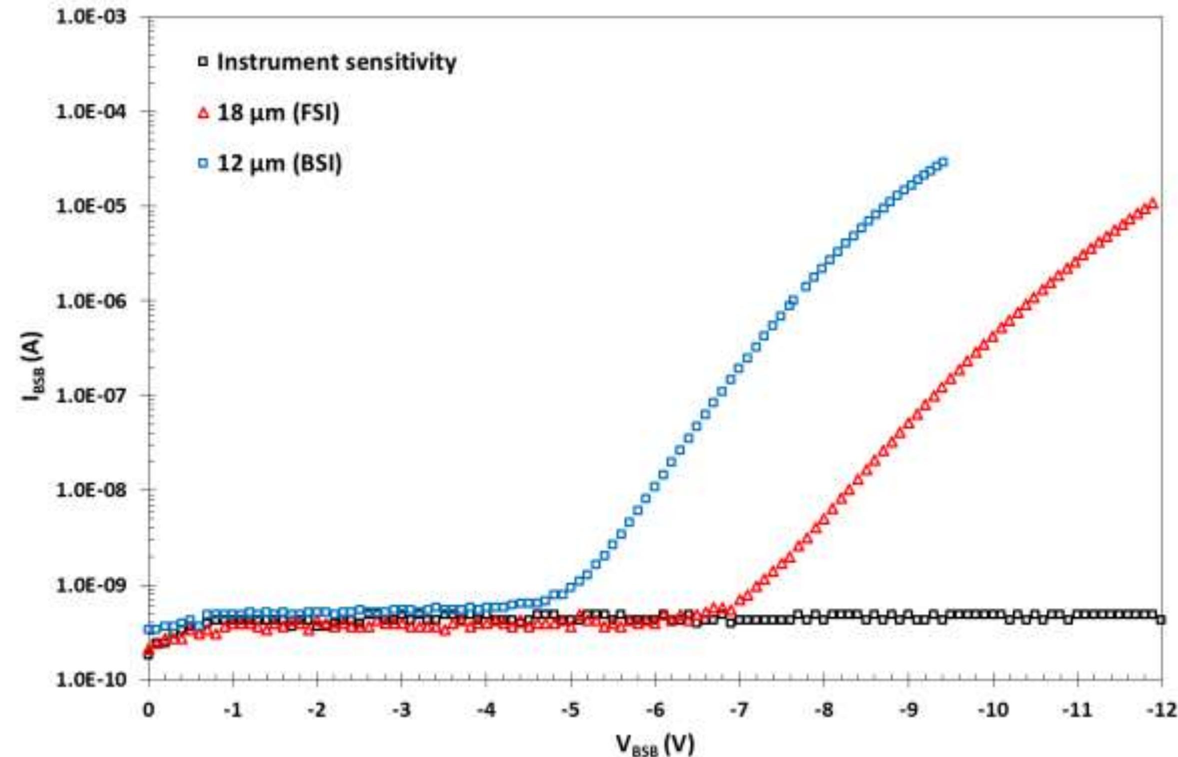


Simulation for high Vpin



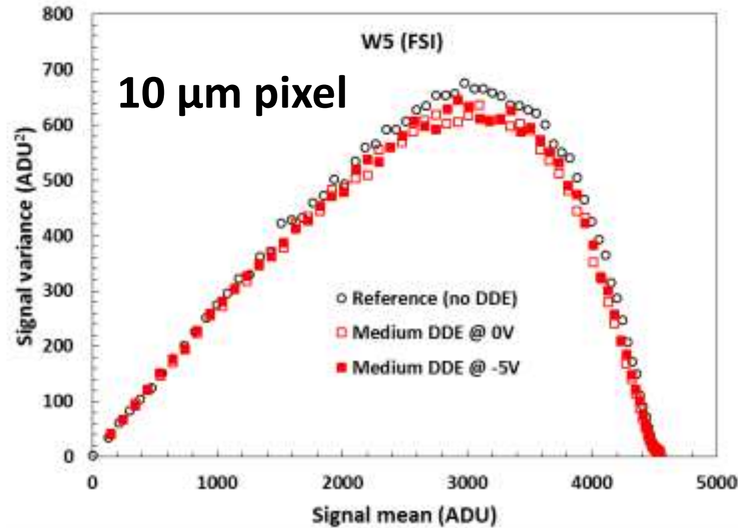
- This shows the reverse current for the whole chip, including the logic and ESD pads
- All pixel variants work
- Reverse bias above -5V with no leakage means that any thickness can be depleted
  - V_{BSB} = -4V fully depletes 18 µm thick epi, 1 kΩ.cm
- Qualitative agreement with the simulations
  - The measurement is for all 8 variants in parallel, simulation is for one variant only

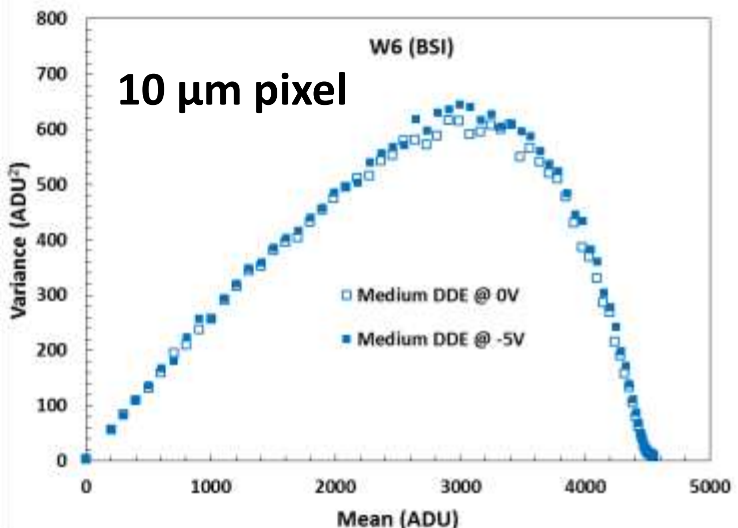
FSI vs BSI chips – reverse voltage



- Epi thickness:
  - FSI = 18 µm
  - BSI = 12 µm
- The reverse bias drops across the fully depleted substrate
- In thinner substrates the potential barrier will start decreasing at lower reverse bias
  - Leakage threshold proportional to epi thickness
  - Measured threshold ratio = 1.44, expected 18 µm/12 µm = 1.5

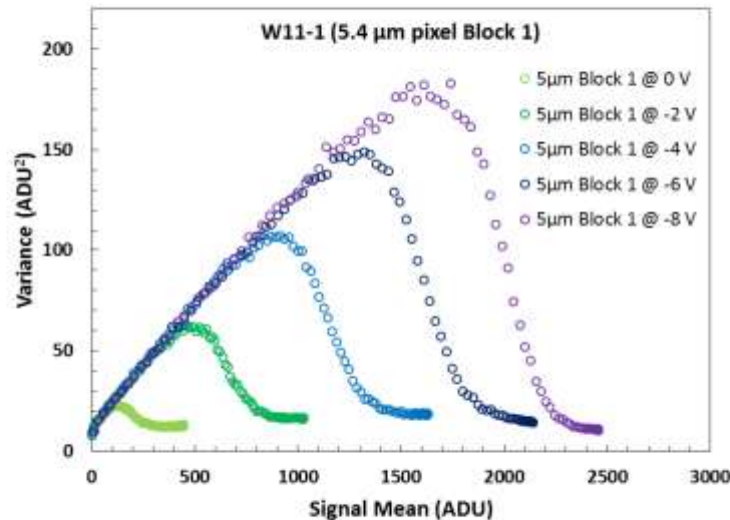
Electro-optical performance

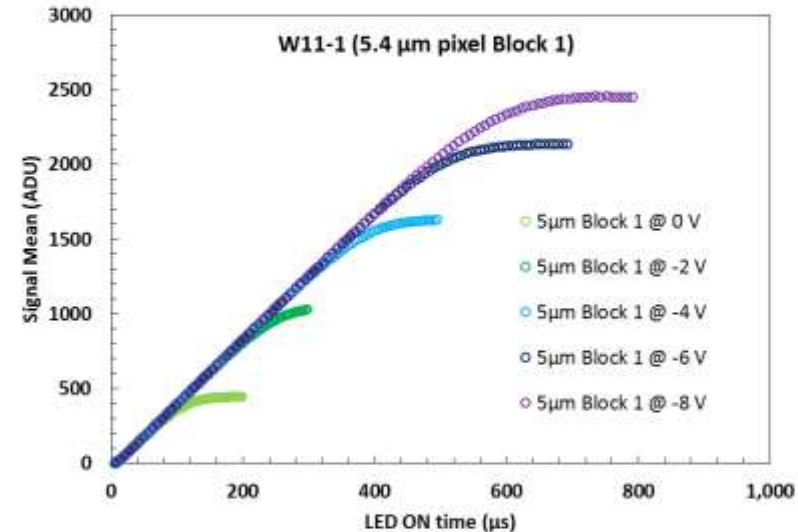




- Photon transfer curves taken under various conditions
- 10 µm pixel:
  - CVF ≈ 80 µV/e- (design = 70 µV/e-)
  - FWC ≈ 15 ke- (design = 20 ke-, limited by the sense node)
  - Noise (in our system) ≈ 8 e- RMS
- 5.4 µm pixel:
  - CVF ≈ 36 µV/e- (design = 33 µV/e-)
  - FWC ≈ 15 ke- (design = 45 ke-, limited by the sense node and off-pixel circuits)
- The new pixels appear identical to the “normal” pixels
- FSI and BSI devices show the same response
- The DDE implant and the reverse bias do not seem to affect the electro-optical performance – great!

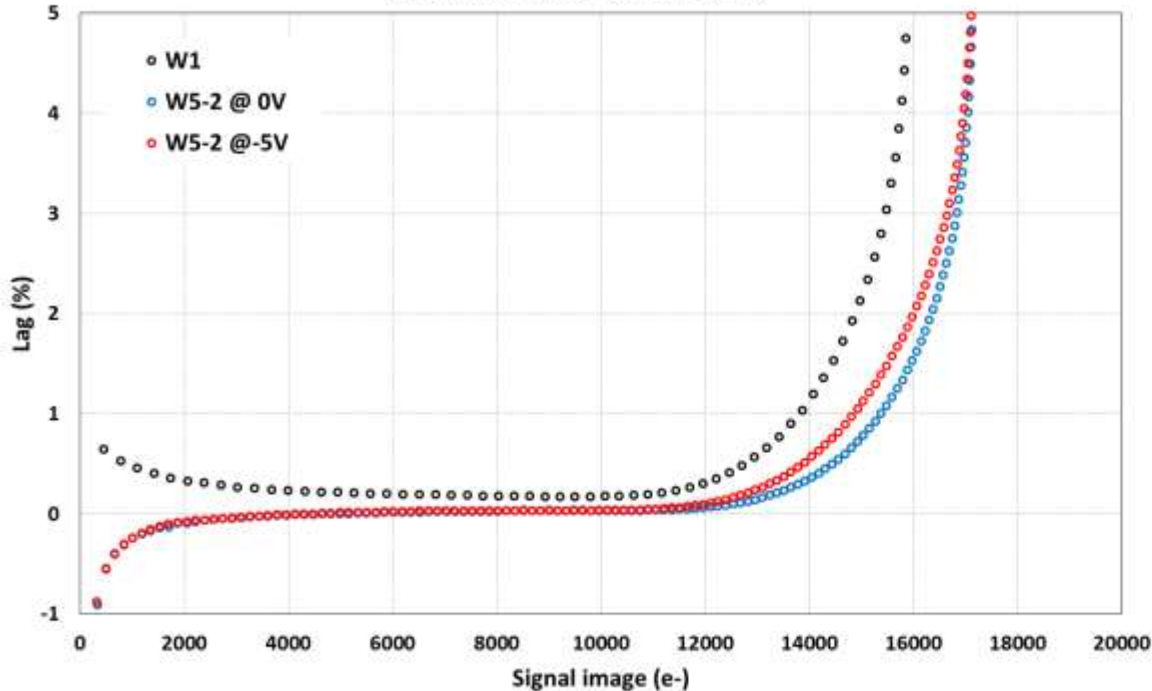
Performance of the 5.4 µm pixel





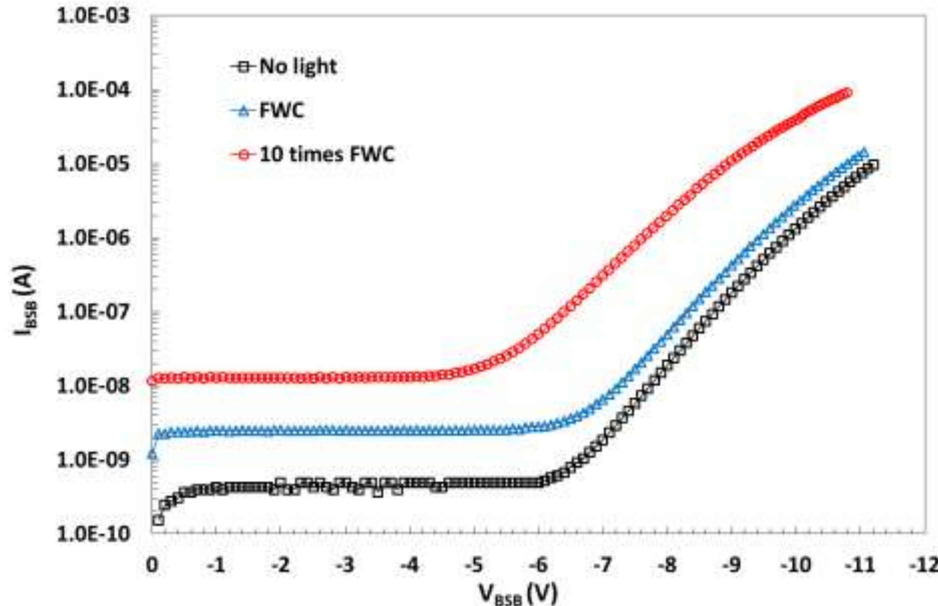
- **Due to constraints in the design the DDE expands under the PPD and the sense node (it avoids the sense node in the 10 µm pixel)**
- **Leads to excessive change sharing, also charge drains away at the array periphery**
- **However, as the DDE potential is reduced by the reverse bias, the DDE becomes less attractive to electrons**
  - **Higher reverse voltage "fixes it"**

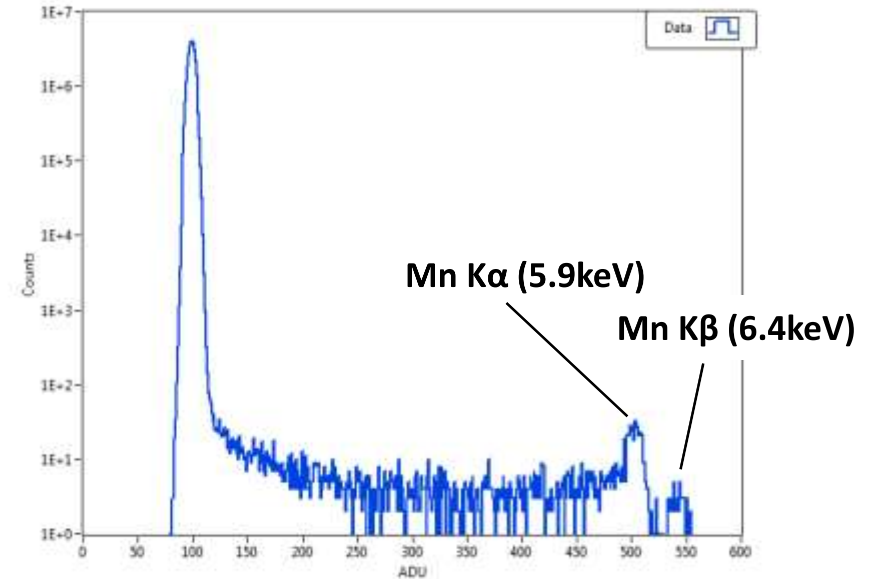
Image Lag



- Image lag is <1% in the original TowerJazz 10 µm pixel
- Lag remains |<1%| in the new design, but changes sign at low signal
  - The reason for this is not understood
- Reverse bias has little effect on lag – good

Performance under strong illumination and X-rays



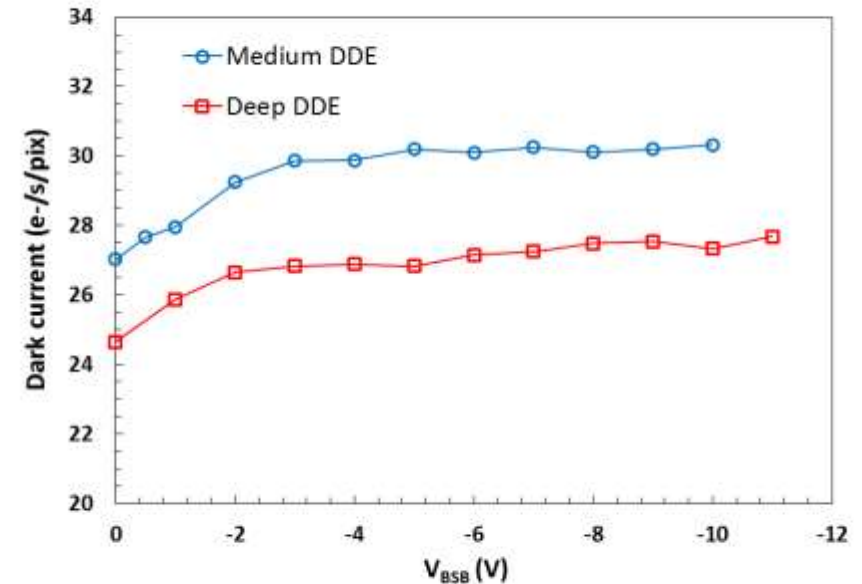


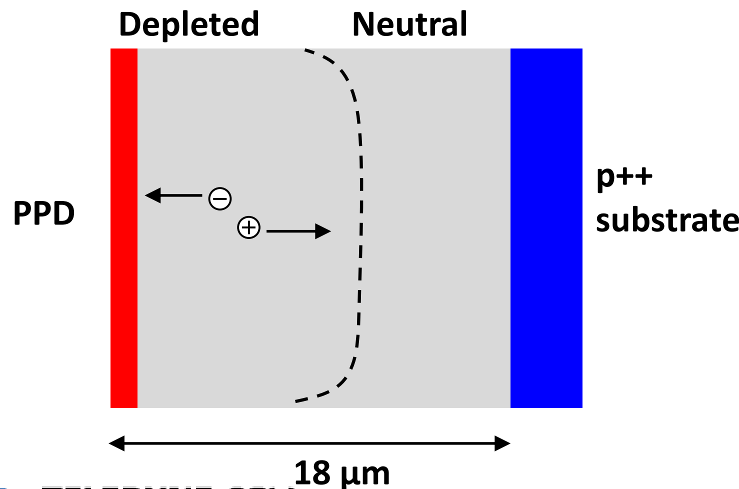
Fe-55 spectrum at -5V reverse bias

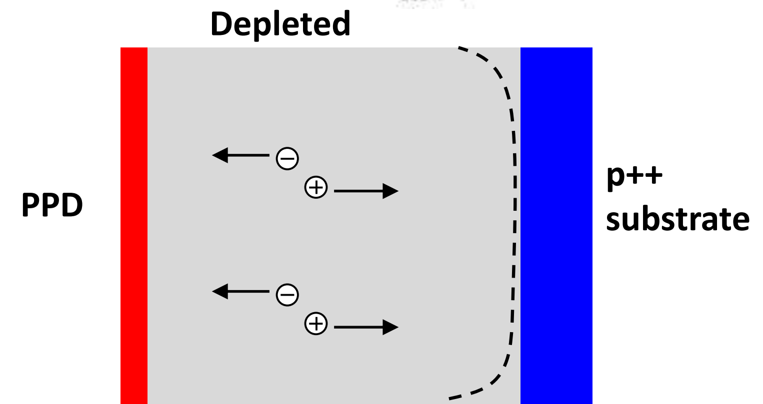
- A concern for strong illumination:
  - PPD potential decreases
  - The pinch-off condition may break down
  - Rise of leakage current
- This was tested with pulsed light
  - No showstoppers
  - Large PPD capacitance and inherent anti-blooming help
- X-ray response is OK, readout noise ~5e- at 500 kHz

Full depletion in FSI chips

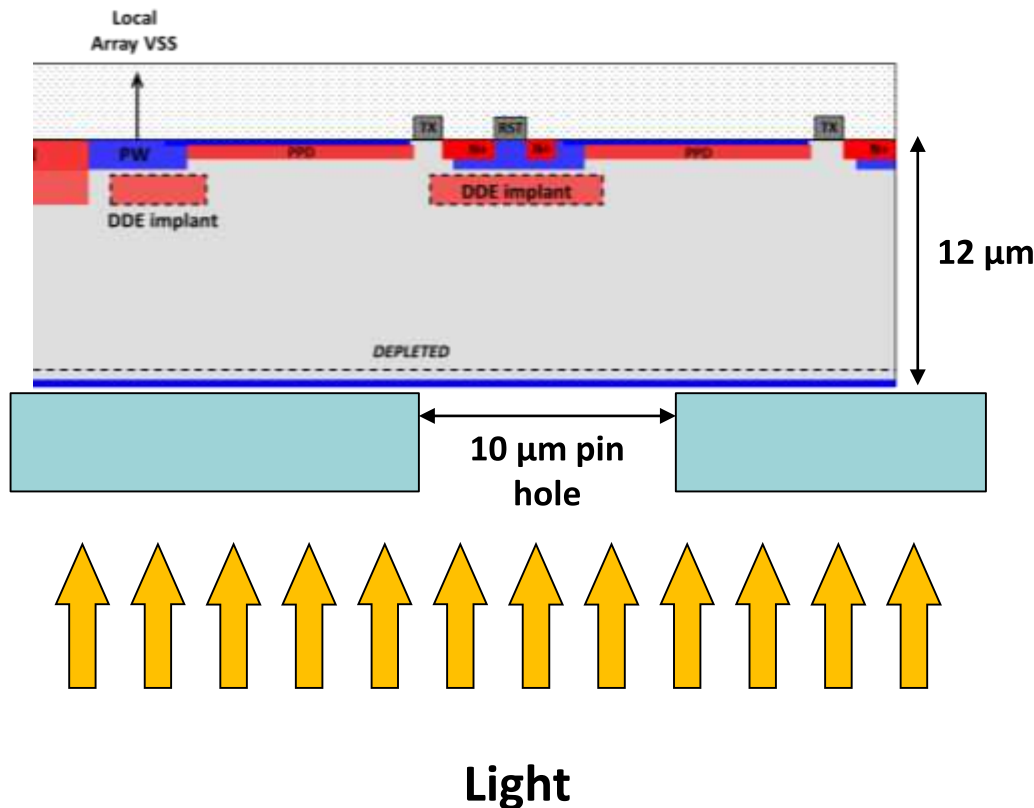
- If there is no reverse current, the device should be depleted
- In front-side illuminated chips:
  - Bulk dark current should increase with the depletion depth
  - Once depletion depth = epi thickness the dark current should level off
  - Expected at V_{BSB} = -4V
- Data shows the expected behaviour, taken as evidence of full depletion





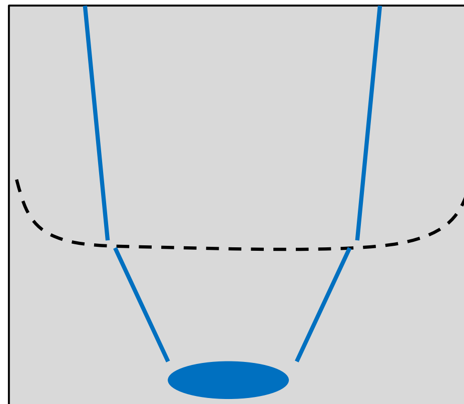


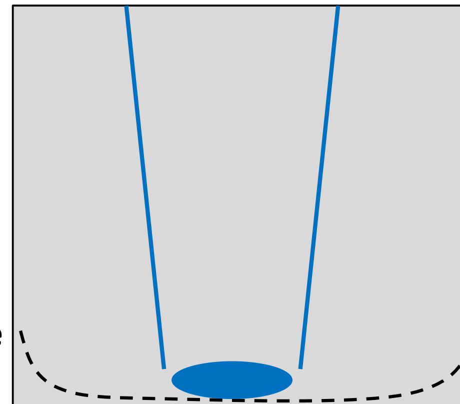
BSI illumination tests

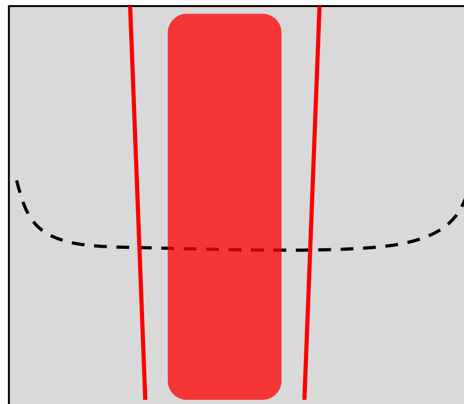


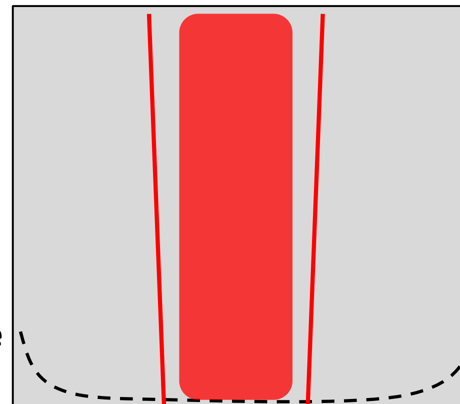
- Two wavelengths:
  - 470 nm (absorption length = 0.6 µm)
  - 940 nm (absorption length = 54 µm)
- Expectations:
  - 470 nm should be very sensitive to the depletion depth, light fully absorbed near the bottom of the device, charge will diffuse more if not depleted
  - 940 nm should not be sensitive because the light is absorbed throughout the device depth.
- Pinhole in contact with the sensor, no optics
- The size of the imaged spot is used as an indication of the depth of depletion

BSI illumination tests



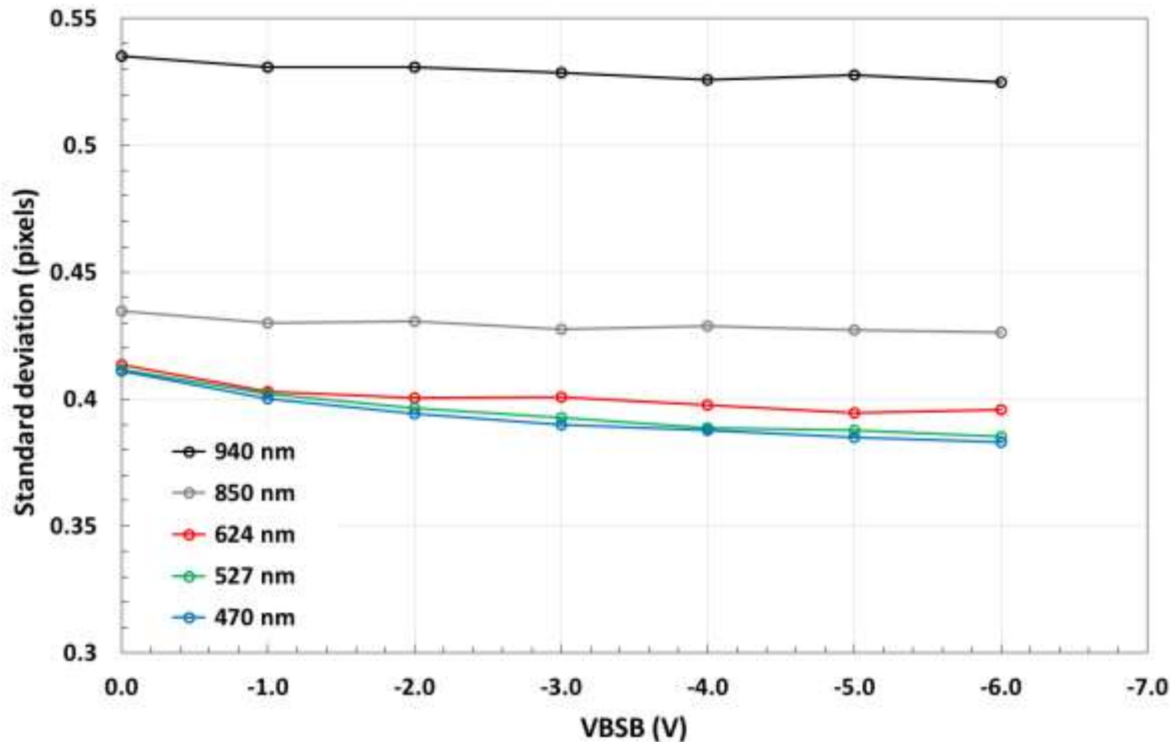






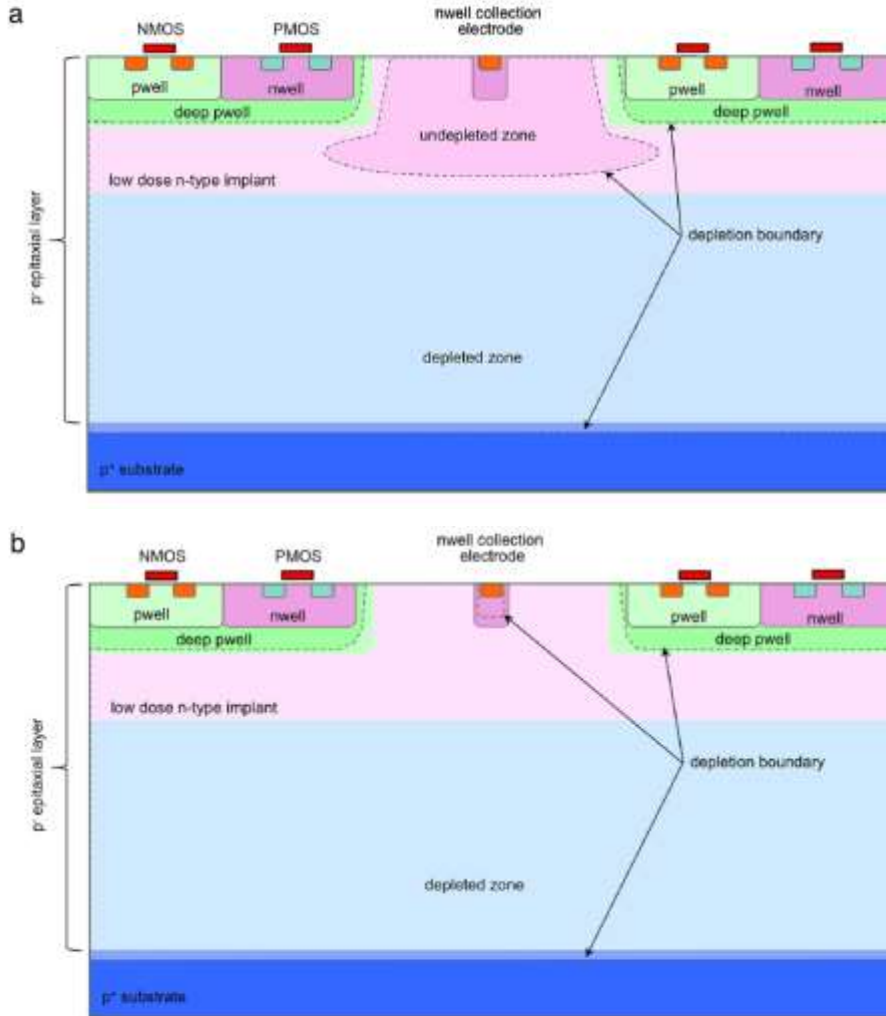
- 470 nm (absorption length = 0.6 µm)
  - Spot should be very sensitive to the depletion depth
- 940 nm (absorption length = 54 µm)
  - Spot should be much less sensitive

Spot size vs reverse bias



- Standard deviation of the spot size in Y direction
  - 470 nm – clear dependence on reverse bias, charge spread is reduced due to increasing depletion
  - 940 nm – little sensitivity on reverse bias
- This is a proof that the reverse bias works.
- The change of the charge spreading is not spectacular due to the epi being only 12 μm thick

Can this principle be used for particle physics?



- Already done!
- Very similar design done at CERN by Walter Snoeys
  - (I was at CERN to show my design in May 2015)
  - TowerJazz had a similar idea at the time
- Here: deep, lightly doped, blanket n-type
  - Under the p-wells
  - Connects to the diode for bias (easier to do than in PPD)
  - Creates a potential barrier
  - Reached reverse bias -15V
- Published in NIM A 871 (2017) 90–96

Summary and plans

- New fully depleted monolithic PPD CMOS sensor using reverse substrate bias
  - First prototype designed on 18 µm, 1 kΩ.cm epi as a proof of principle
  - Can be scaled to much thicker epi/bulk substrates
  - Both FSI and BSI devices manufactured
  - Patent-pending
- Can be attractive to a large number of applications
  - Could offer high QE on a par with thick CCDs and hybrid CMOS
  - Low noise, monolithic CMOS design, radiation hard, low power
- Very successful development – objectives met on the first attempt
- Two papers (one in IEEE Electron Device Letters) published
  - Presented at the International Image Sensor Workshop (May 2017), best poster award
  - At least one more paper to be written (invited to publish in Sensors by IISS)
- Next steps – produce a full scale imager and industrialise
  - Larger device on 40µm epi
  - Small device on bulk higher resistivity silicon – could be >100µm thick

First peer-reviewed paper published

64 IEEE ELECTRON DEVICE LETTERS, VOL. 38, NO. 1, JANUARY 2017

Fully Depleted Pinned Photodiode CMOS Image Sensor With Reverse Substrate Bias

Konstantin D. Stefanov, *Member, IEEE*, Andrew S. Clarke, and Andrew D. Holland

***Abstract*— A new pixel design using fully depleted pinned photodiode (PPD) in a 180-nm CMOS image sensor (CIS) process has been developed and the first experimental results from a test chip are presented. The sensor can be fully depleted by means of reverse bias applied to the substrate, and the principle of operation is applicable to very thick sensitive volumes. Additional n-type implants under the in-pixel p-wells have been added to the manufacturing process in order to eliminate the large parasitic substrate current that would otherwise be present in a normal device. The new design shows the same electro-optical performance as the PPD pixel it is based on, and can be fully depleted without significant leakage currents. This development has the potential to greatly increase the quantum efficiency of scientific PPD CIS at near-infrared and soft X-ray wavelengths.**

***Index Terms*— CMOS image sensor (CIS), pinned photodiode (PPD), full depletion, reverse bias.**

I. Introduction

CMOS image sensors (CIS) based on the pinned photodiode (PPD) [1] are widely used today in high performance imaging. For scientific imaging, for example in astronomy and X-ray detection, hybrid CIS and backside-illuminated (BSI) sensor [4], however due to the lateral charge diffusion during the increased transit time the spatial resolution deteriorates [6]. The magnitude of the reverse bias depends on the resistivity and the thickness of the semiconductor substrate and can far exceed any other voltage in the system. The structures of both hybrid CIS and CCDs appear as reverse biased pn junctions, and this allows operation without undesirable leakage currents.

Fig. 1. Cross section of the proposed 4T PPD pixel design along the central line of charge transfer and the reverse biasing structure. The two readout transistors T1 and T2 are physically situated in the p-well, and the reset transistor is formed between the reset drain (RD) and the sense node.

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The Best Poster Award is given to the best poster of the workshop as voted by the workshop attendees

Year	Paper	Primary author	Co-authors	Affiliation
2017	Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias	Konstantin D. Stefanov	Andrew S. Clarke, James Ivory and Andrew D. Holland	The Open University, UK
2015	Analysis and Reduction of floating Diffusion Capacitance Components of CMOS Image Sensor for Photon-Countable Sensitivity	Fumiaki Kusuhara	Shunichi Wakashima, Satoshi Nasuno, Rihito Kuroda and Shigetoshi Sugawa	Tohoku University
2013	Digital Integration Sensor	Song Chen	A. Ceballos, and E.R. Fossum	Dartmouth
2011	Photo-Sensitive Area Modulation Pixel for 3D Real-Time CCD Imager	Y. Hashimoto	F. Kurihara, K. Murakami, K. Imai, K. Taniguchi	Matsushita and Osaka Univ.
2009	Investigating the Ageing Effects on Image Sensors Due to Terrestrial Cosmic Radiation	Gayathri G. Nampoothiri	Albert J.P. Theuwissen	Delft Univ. and Harvest Imaging