TWEPP 2015 - Topical Workshop on Electronics for Particle Physics

Overview by

Stephanie Sullivan

TWEPP Workshop

- Lisbon, Portugal
- 28 Sept – 2 Oct
- 226 participants
- More of a conference than a workshop

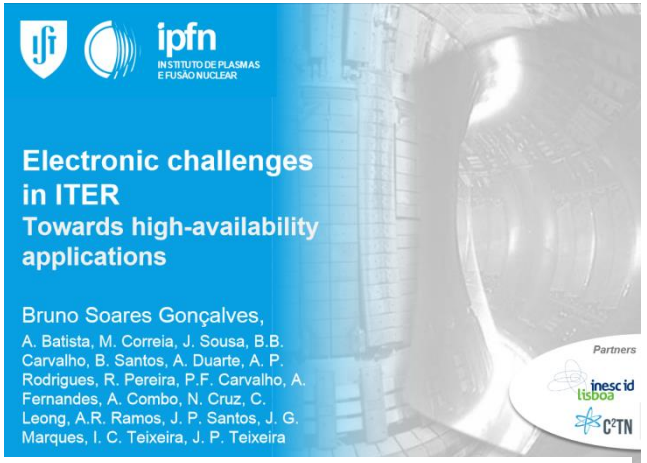
- Full presentations:
- https://indico.cern.ch/event/357738/timetable/#20150928.detailed

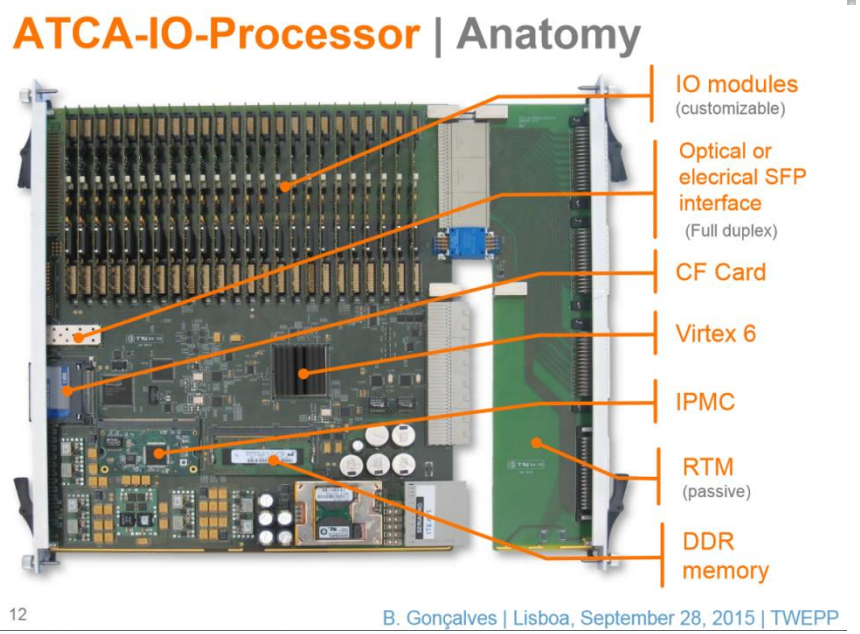
Particle Physics in Portugal

- Professor Rogerio Colaco
- Portugal joined CERN in 1985/86
- Rapid expansion in physics research in Portugal over the last 30 years.

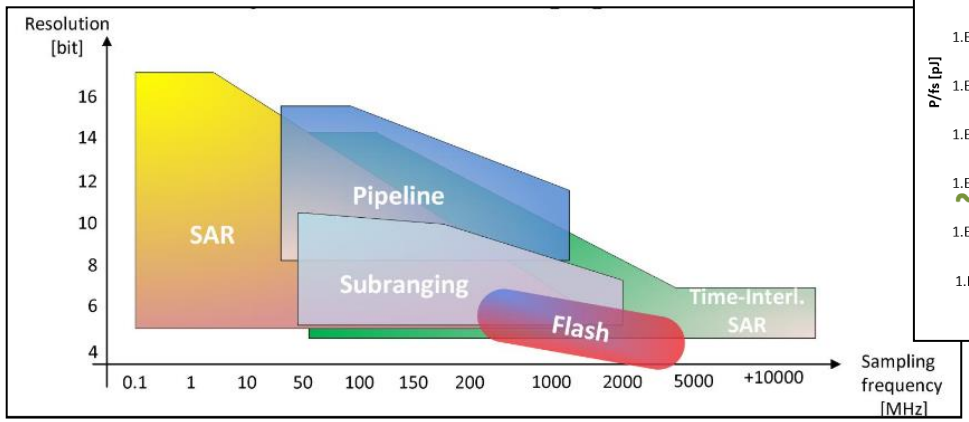
Control in Fusion Plasmas

- High speed, high reliability, high availability, high data volume
- Using ATCA boards for very high data volumes
- Not clear what was custom and what is COTS





- **Good reference for ADC architecture trade off studies.**
- Energy efficiency vs SNR over time has improved.
- Tradeoffs:
  - Speed
  - Resolution
  - Power consumption



High-Performance Analog-to-Digital Converters: Evolution and Trends

Pedro Figueiredo

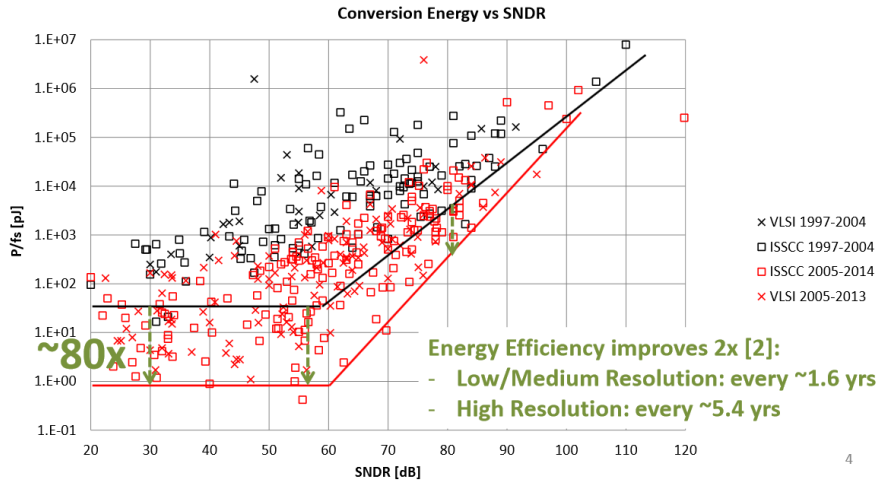
pmff@synopsys.com

Topical Workshop on Electronics for Particle Physics 2015

28th September 2015

Evolution of ADC performance

- Data from Prof. Murmann's Survey [1]



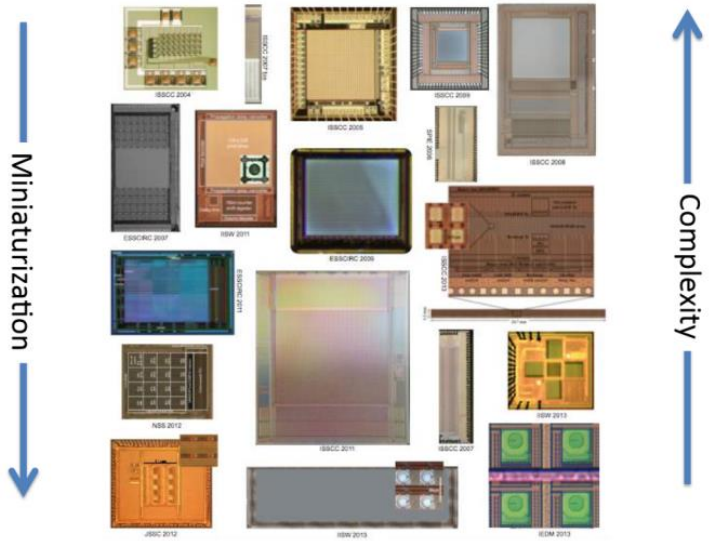
Status and Future Prospects of High Time Resolution Photon Counting Sensor Arrays

A decade of CMOS photon counting & single-photon imaging (2004-2015)

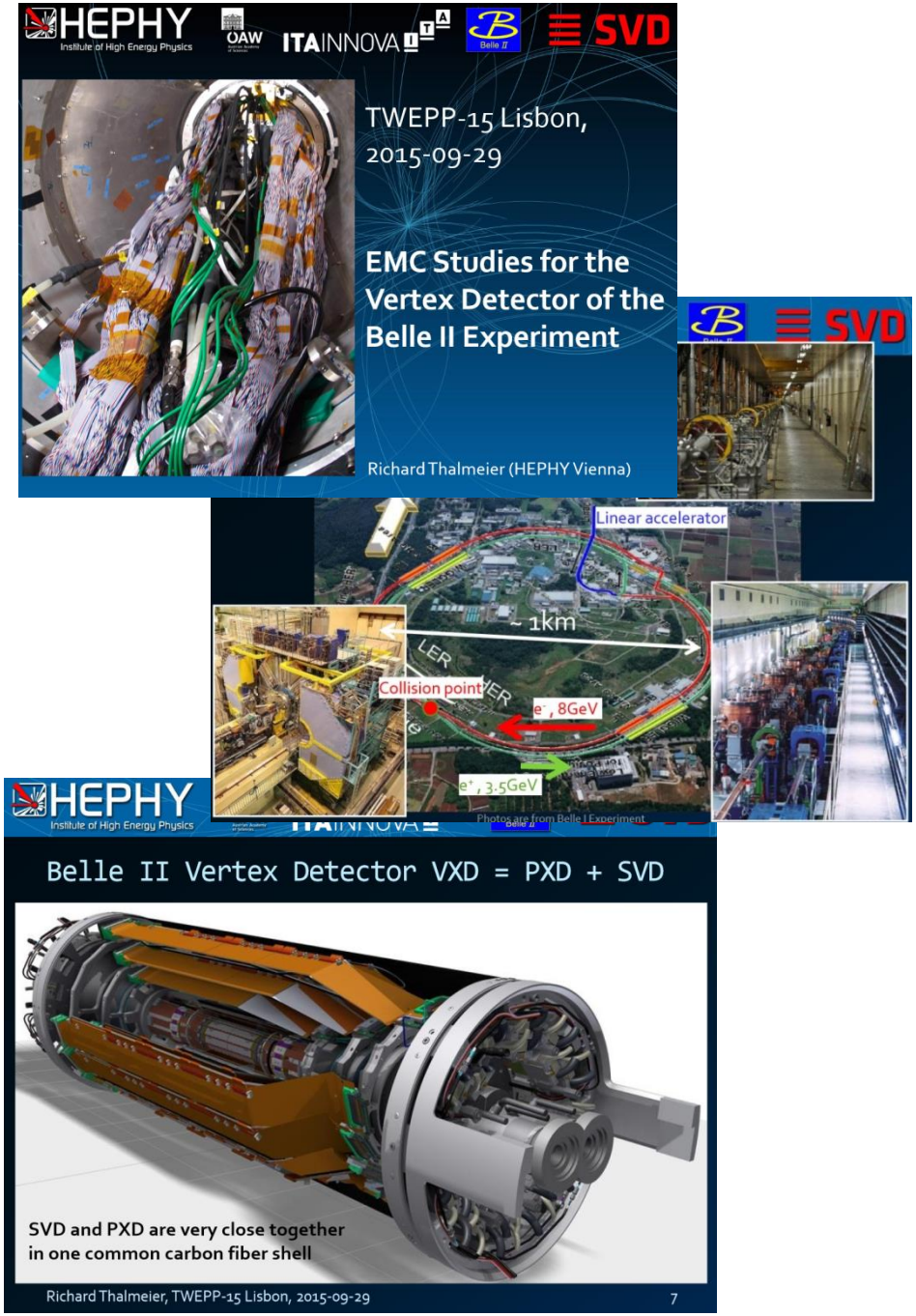
E. Charbon

TU Delft

All-Digital Imagers based on Single-Photon Detection (2004-15)

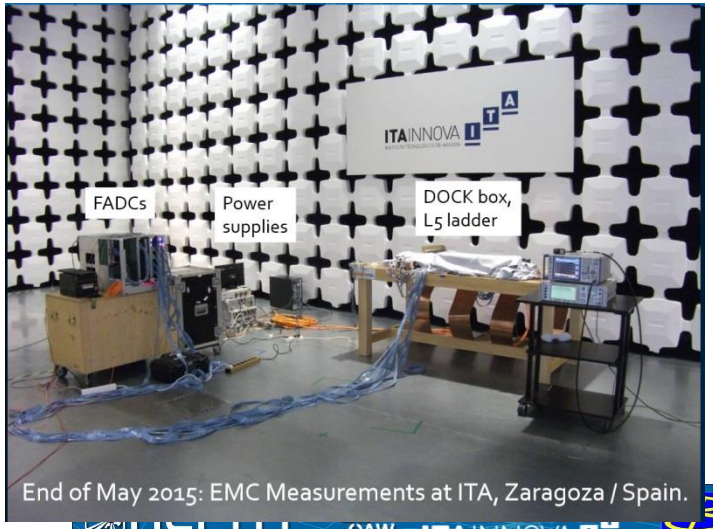


- Multiple single photon detectors already exist
- Talk focused on Single Photon Avalanche Diodes
- Increasing sensitivity increases noise
- Multiple projects for medical imaging

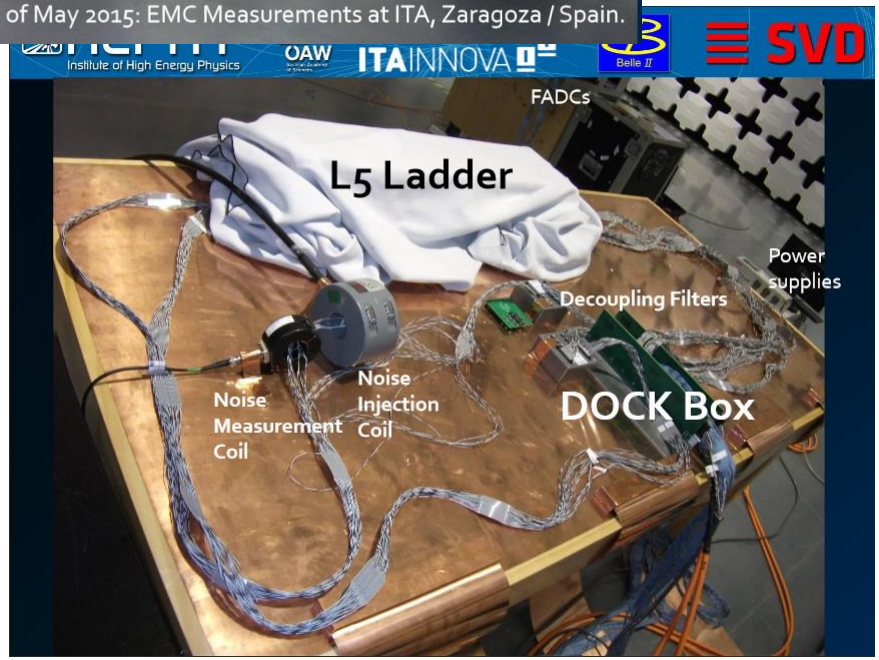


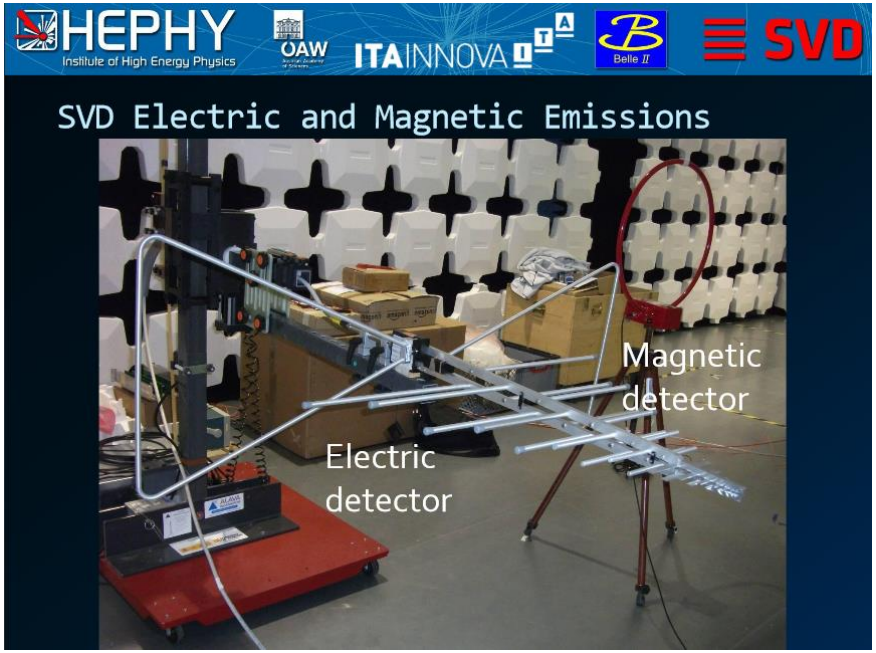
- Pixel Detector (PXD) and Silicon Vertex Detector (SVD) share cable tunnels
- SVD worked alone
- Installing PXD caused noise problems in SVD, even when PXD off.
- Grounding “some points” to magnet housing helped
- **More info on EMI issues.**

Belle II cont.



- ITA facility in Spain has ability to test EMI issues of cables and boards.





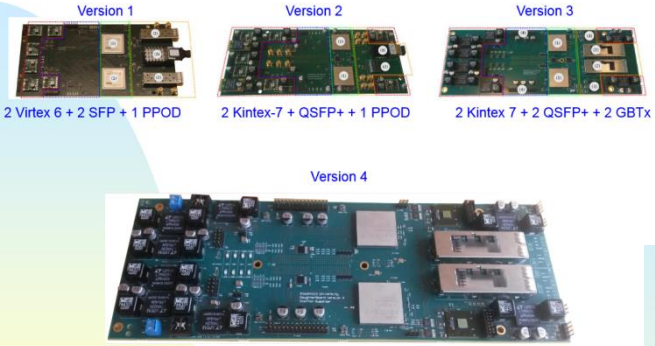
A radiation tolerant Data link board for the ATLAS Tile Cal upgrade

H. Åkerstedt, C. Bohm, S. Muschter, S. Silverstein and E. Valdes
On behalf of the ATLAS Tile Calorimeter System

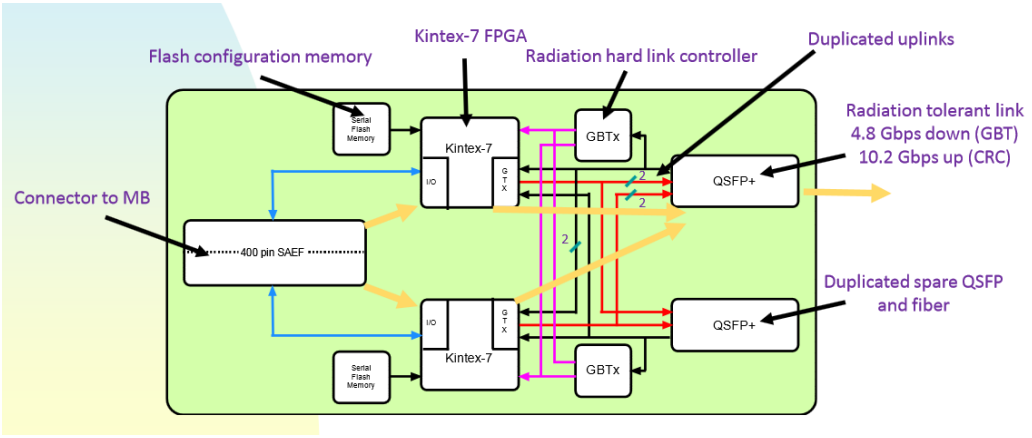
Outline

ATLAS TileCal
Upgrade aims
Overview of the Phase II upgrade
The Data link board
The Upgrade Demonstrator

Link Board history



- Using GBTx for downlink, but not uplink.
- Not sure why GBTx is used this way.
- Design is to reduce effects of SEU's.
- Lots of redundancy.



Past and Future of Microelectronics in HEP

A roadmap for R&D in microelectronics for Detector Builders

A. Marchioro
CERN/PH-ESE

50th anniversary of G. Moore's paper

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

machine instead of being concentrated in a c
addition, the improved reliability made possibl
circuits will allow the construction of larger pr
Machines similar to those in existence today
around.

mean all the
microelectr

4

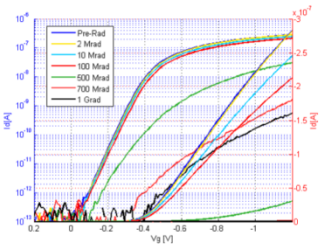
Technologies around the corner

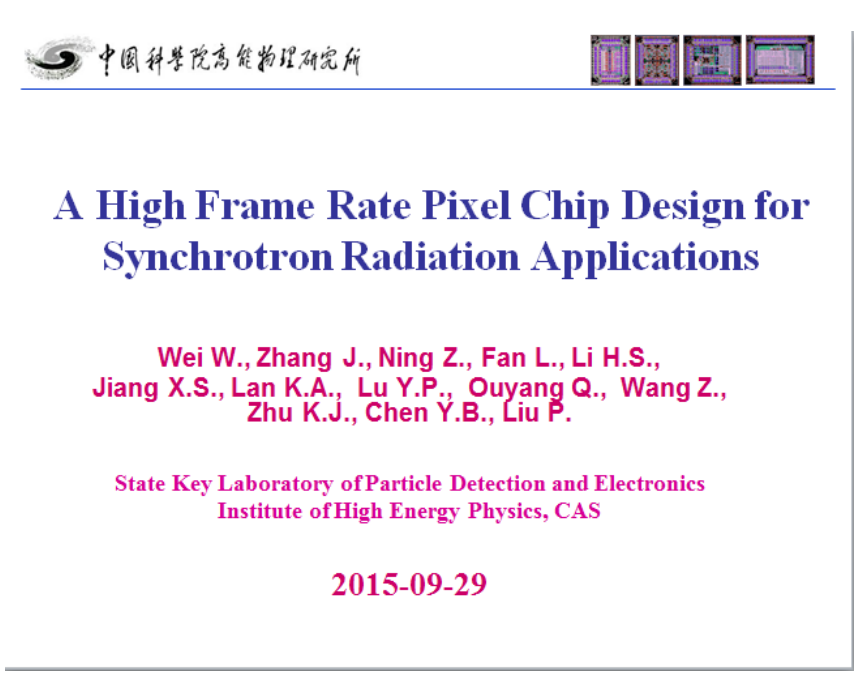
- FinFet
- FDSOI
- TSVs
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non kT/q controlled thresholds slopes

- Industry focused on cheaper transistors, not necessarily smaller ones (though it tends to be the same thing).
- Cost per transistor still going down.
- Size of transistor in 2D is approaching physical limits.

Can 65nm survive 1 GRad

- Issue is much more complex than RH of ¼ um in 1996
- Discordant effects related to:
  - N/P
  - Total dose
  - Dose rate
  - Size of devices
  - Temperature
  - Biasing conditions
  - Interplay of items above
- RH > Grad is unlikely to be relevant outside HEP
- R&D Investment (manpower) required >> than what was done previously.
- See talk of Federico @ MUG





- Sensor and ASIC fully designed and built in China
- University and industry partners.

Polyurethane spray coating of aluminum wire bonds to prevent corrosion and suppress resonant oscillations

J.M. Izen, R. Boyd*, M. Kurth

*Univ. of Oklahoma

Introduction and Goals

Unencapsulated aluminum-wedge wire bonds are common in pixel and strip detectors.

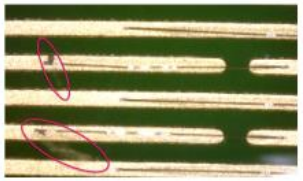
Bulk bond encapsulation traditionally eschewed due to thermal expansion and radiation concerns.

Wire bond problems are a persistent failure mode:

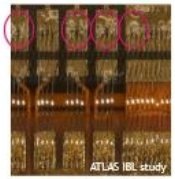
- Condensation-induced corrosion, particularly when Cl^- present.
- Periodic Lorenz forces at wire bond resonance frequency can break bonds.

Goals: Perfect PU spray-coating techniques. Evaluate PU coating corrosion resistance and the protection PU affords against resonant driving forces. Qualify PU for use with the ATLAS ITK Pixel detector, first at room temperature, and then at -20 C

Halide-Catylized Corrosion: $Al + 3H_2O \rightarrow Al(OH)_3 + 3H_2 \uparrow$



Aluminum wire bonds in deionized (DI) water. Hydrogen plumes and bubbles visible



White corrosion residue visible with low-angle lighting. Traces of chlorine detected on ENIG surface

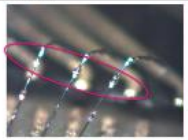
- QARTlab test: DI water test provokes corrosion in 6 of 8 PC boards sampled from CERN experiments and labs [1]
- Condensation/corrosion prior to and during quality assurance testing, particular for tests requiring cooling [2]
- Corrosion risk appears to be a common concert.

Application of Polyurethane Coatings

Polyurethane: Cellpack D 9201 Urethane
Spray can and bulk liquid
Formulated for electrical insulation and corrosion resistance

Spray can results unusable
Uneven blobs on bond wires in every attempt

No control of droplet size and flow rate



PU coating from a spray can

Paasche Talon Dual Action Airbrush TG2L

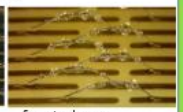
Art-Supply Air Brush

- Better control of pressure, flow, nozzle size
  - Smaller droplet size in atomized spray
  - Some control over droplet size
  - Coating build-up in several passes
- Nozzle + needle can be cleaned
- Smaller painted region
  - Further collimation of spray possible with a mask
- Use liquid Cellpack D 9201 PU, 0.65mm nozzle

Polyurethane-coated 25 μ Al wire bonds

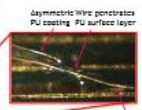
Spray too fine: droplets partly dry before reaching wire.

Goldilocks spraying
Smooth, hermetic coatings
~35μ to ~100μ outer diameter



Spray too heavy.
Droplets

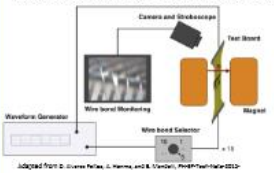
Tens of spray passes build up desired PU thickness



Periodic Lorenz Force: Intermittant Current in a B Field

- Resonant oscillations broke wire bonds on CDF silicon tracker [3]
- ATLAS Pixel protects disk LV power wire regulator wire bond heels by potted with Dymax
- ATLAS SCT and IBL: software prevents readout in resonance frequency range

- Goal: survive 100 mA p-p, B = 2T, at wire bond resonant freq.



B=1.5-1.7 T 50% duty square wave 0 - 180 mA p-p
Worst-case (end cap/disk) geometry Test 25μ, 2.8 mm long bond wires at f_{res}

Sample	f_{res} [kHz] mean, range	Q mean, range	$I_{p\text{-}p}$ [mA] to break
2.8 mm uncoated PCB C3, N_{xtrac}=17	11.78 (11.68 -11.97)	92 (69 - 117)	4 one wire
2.8 mm potted PCB D2, N_{xtrac}= 8	14.95 (13.80 - 16.17)	68 (60 - 77)	12 - 15 one wire
2.8 mm PU light PCB C10, N_{xtrac} = 15	9.28 (8.88 - 9.76)	36 (26 - 46)	32 - 40 one wire
2.8 mm PU heavy PCB C9, N_{xtrac}= 8	(8.1 - 14.1)	(7 - 14)	f_{res} = 10.4 kHz: breaks @ 180 mA p-p f_{res} = 13.3 kHz: 38.5 hours @ 180 mA p-p 1.7 T

As PU coating thickens,
- f_{res} decreases to ~8 kHz due to increasing mass
- Then f_{res} increases due to mechanical stiffness of PU
- Energy absorption from flexing PU decreases Q-factor
- Best protection when f_{res} > 12 kHz

4 "bullet-proof" 2.8mm wires survive B=1.7 T, disk geometry, $I_{p\text{-}p} \geq 180$ mA, > 1 h
- f_{res} = 12.1, 13.5, 11.3, 13.3 kHz

Mechanical energy absorption by PU flexing reduces Q-factor and oscillation amplitude

First irradiated sample 27 MeV protons: 0.94 × 10^{14} 1 MeV n_{eq}/cm^2 = 10.3 MGy)
Maximum Expected ITK Pixel Dose: Inner Barrel 7.7 MGy 1st Disk - 0.9 MGy [4]

Sample B3 ~100μ OD	Before Irradiation		After Irradiation		
Wire Number	f_{res} (Khz) ±0.1	$Q_{Ba/Fe/w}$ ±7%	f_{res} (Khz) ±0.1	$Q_{Ir/Fe/w}$ ±7%	$Q_{Ba/Fe/w}/Q_{Ir/Fe/w}$ ±10%
2	9.8	15.0	11.3	35.9	2.4
3	9.8	12.5	11.6	32.1	2.6
4	9.9	15.1	11.9	33.0	2.2
10	12.8	12.2	16.2	32.5	2.7
12	13.5	14.7	17.1	31.7	2.2
13	13.5	12.1	16.9	34.9	2.9
15	12.5	13.6	16.7	40.3	3.0
16	11.4	14.3	13.7	30.3	2.1

- Increase in f_{res} and Q consistent with radiation curing of PU and some loss of flexibility

Status and Conclusions

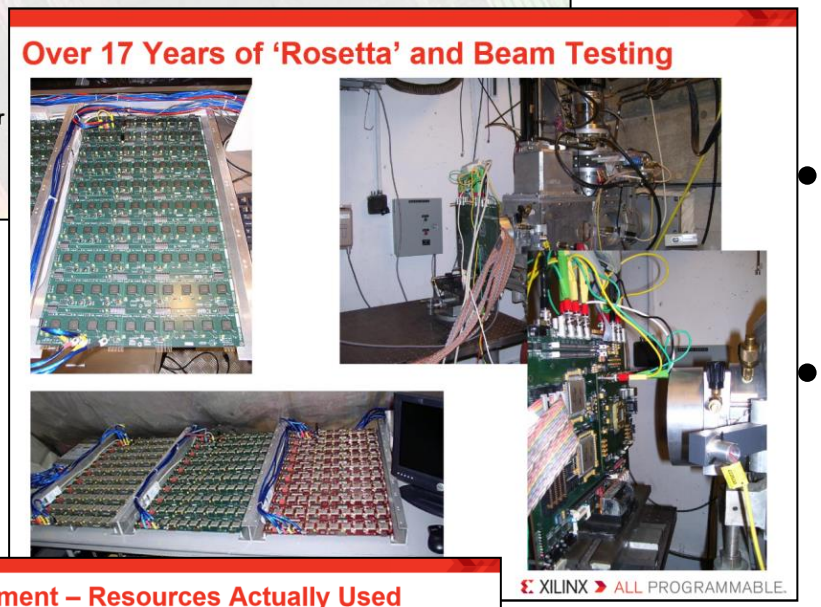
- Acceptable PU coatings achieved
- Corrosion and resonance protection at room temperature demonstrated
- PU a co-polymer of polyisocyanate and a polyol such as polyether or polyester.
  - Chain length affects flexibility
  - Explore formulations developed for flexibility
- Study thermal expansion damage as a function of thickness.
  - ITK Pixel Endcap/disk wire bonds may prefer a thicker PU coat that ITK Pixel Barrel

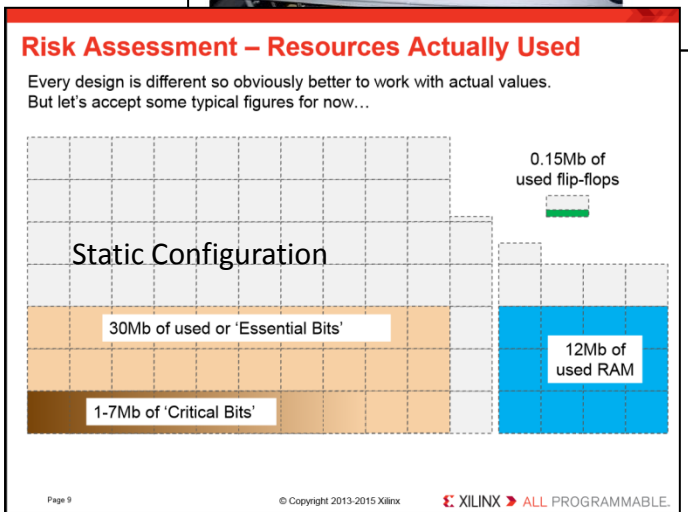
References

[1] A. Honma, F. Manolescu, I. McGill, https://indico.cern.ch/event/283860/contribution/1/attachments/523708/722352/status_report_honma_18nov2013.pdf, p.6.
[2] Atlas Collaboration, Atlas Pixel IBL: Stave Quality Assurance, 2014, CERN, ATL-INDET-PUB-2014-006, https://cds.cern.ch/record/1754309/files/ATL-INDET-PUB-2014-006.pdf
[3] G. Bolla et al., Nucl. Instr. and Methods A518, 277 (2004)
[4] ATLAS Letter of Intent - Phase II Upgrade, https://cds.cern.ch/record/1502664/files/LHCC-I-023.pdf

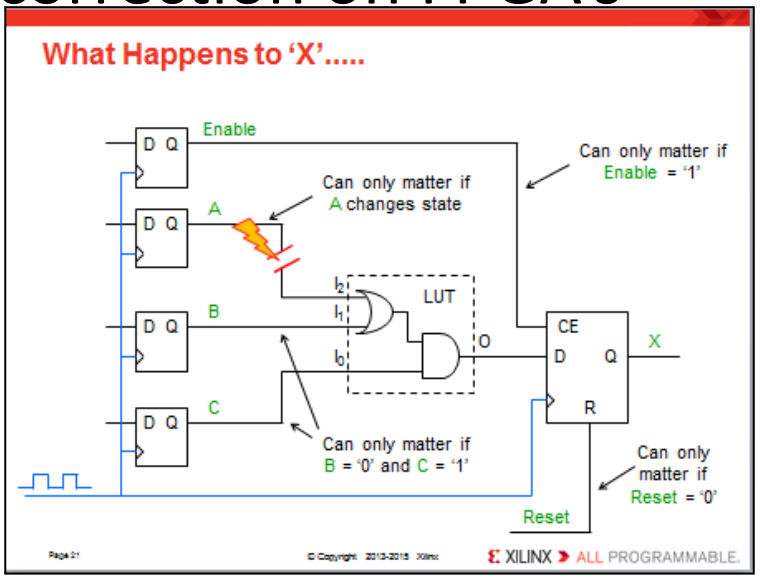
Acknowledgements

Thanks to the staff of CERN's Departmental Silicon Facility: A. Honma, F. Manolescu, and I. McGill for





- Xilinx reliability data
  - http://www.xilinx.com/support/documentation/user_guides/ug116.pdf
  - See the slide notes, too.
- New chip will have lower SEU rates.
- Xilinx has code for error correction on FPGA's

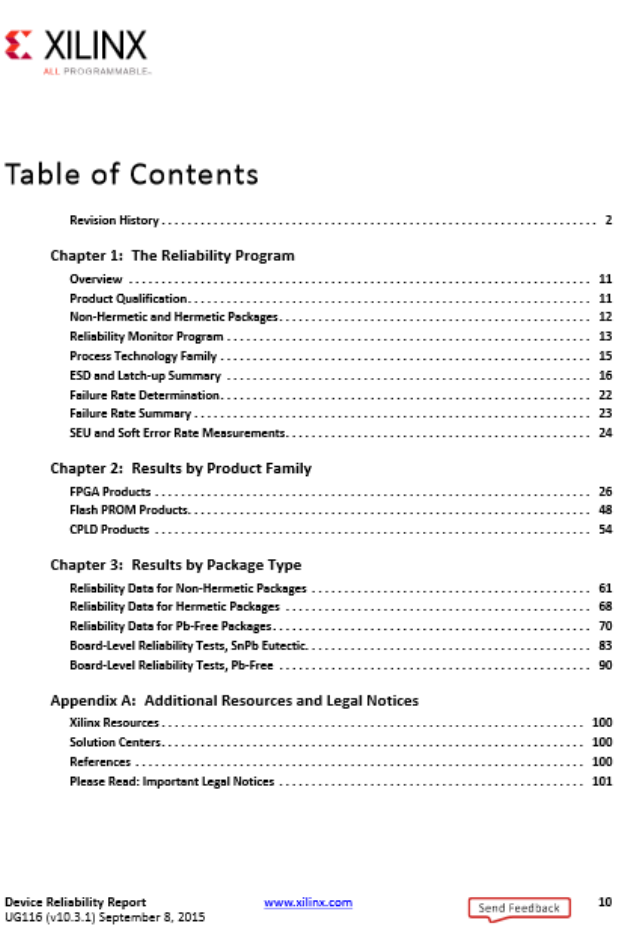


Xilinx Side Meeting

- Reliability testing used to be done in Dublin.
  - Just moved to Taiwan
- Speaker based in Surrey
- Willing to work with us on reliability studies, when goals align
- Defence grade Xilinx parts are not ITAR restricted

Xilinx UG 116 – Reliability Report

- http://www.xilinx.com/support/documentation/user_guides/ug116.pdf
- Publicly released reliability data
- Details on test conditions and failure rates
- Most tests are 1000h

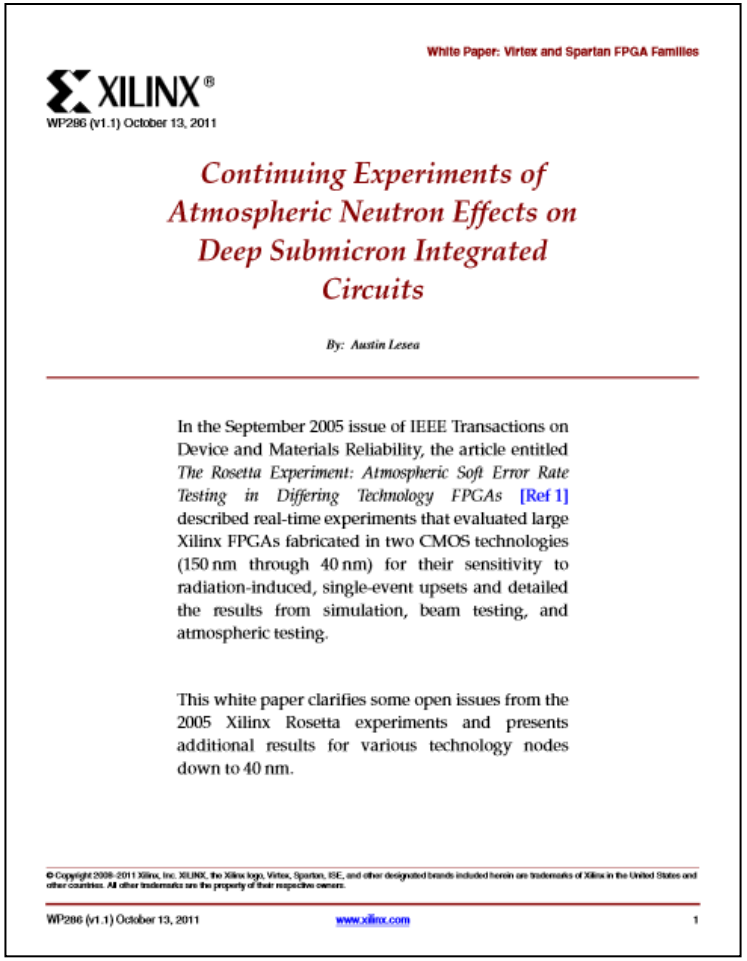


XILINX
ALL PROGRAMMABLE.

Table of Contents

Xilinx WP286 – SEU Study

- http://www.xilinx.com/support/documentation/white_papers/wp286.pdf
- Long-term FPGA testing
- Measurable difference in upset rate due to low alpha lead vs normal lead



White Paper: Virtex and Spartan FPGA Families

XILINX®

WP286 (v1.1) October 13, 2011

Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits

By: *Austin Lesea*

In the September 2005 issue of IEEE Transactions on Device and Materials Reliability, the article entitled *The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs* [Ref 1] described real-time experiments that evaluated large Xilinx FPGAs fabricated in two CMOS technologies (150 nm through 40 nm) for their sensitivity to radiation-induced, single-event upsets and detailed the results from simulation, beam testing, and atmospheric testing.

This white paper clarifies some open issues from the 2005 Xilinx Rosetta experiments and presents additional results for various technology nodes down to 40 nm.

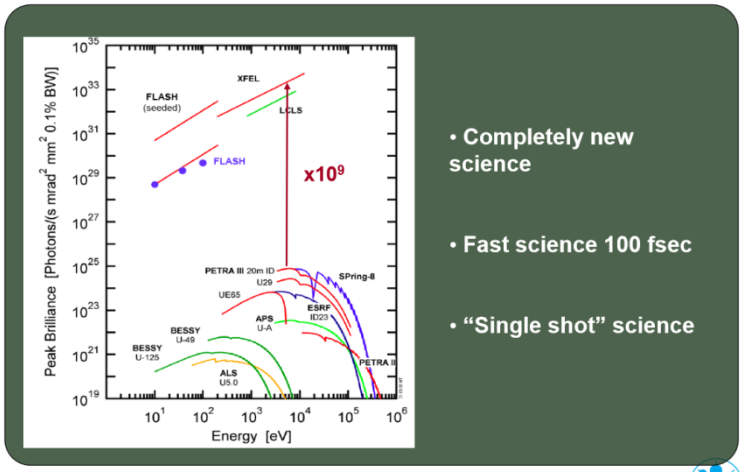
Detector Developments at DESY for Free Electron Lasers.

Heinz Graafsma,

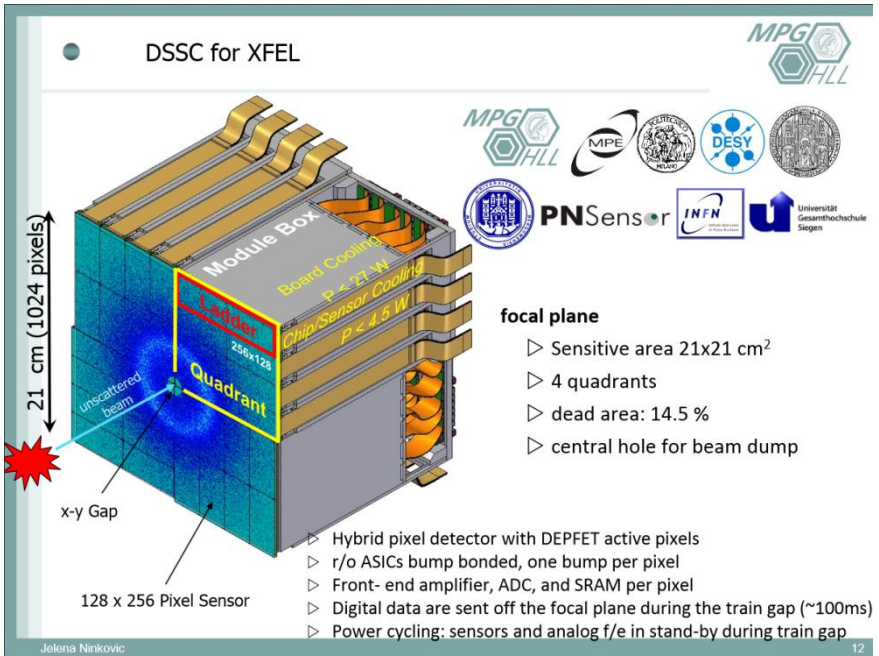
DESY-Hamburg Germany &
University of Mid-Sweden

- High dynamic range
- Single photon sensitivity
- Fast response
- Rad hard
- Can look directly at beam of existing lasers, only scattering from XFEL

The XFEL-Challenge: Different Science



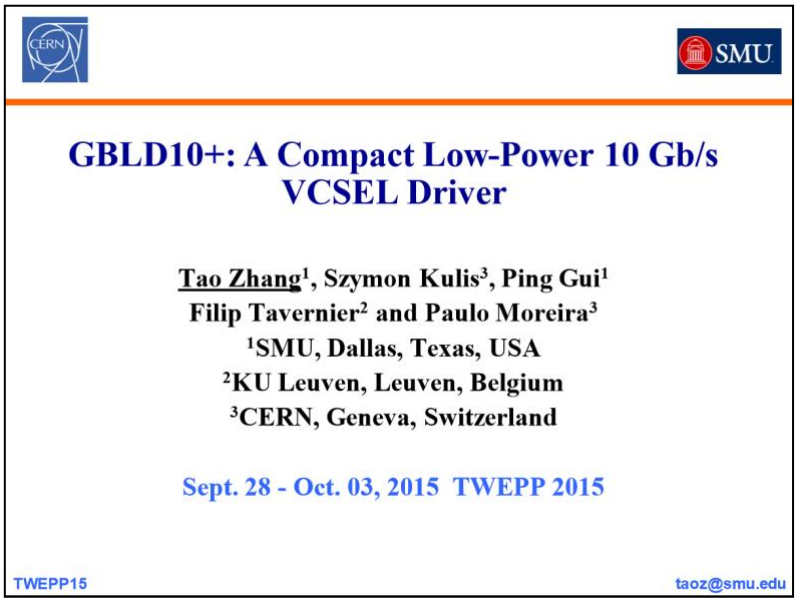
- Completely new science
- Fast science 100 fsec
- "Single shot" science

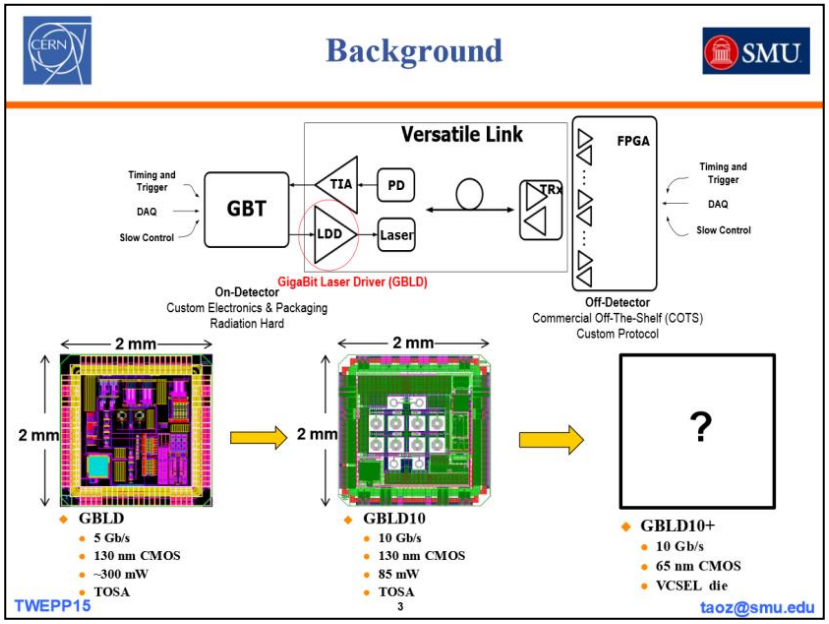


Electronics Qualification

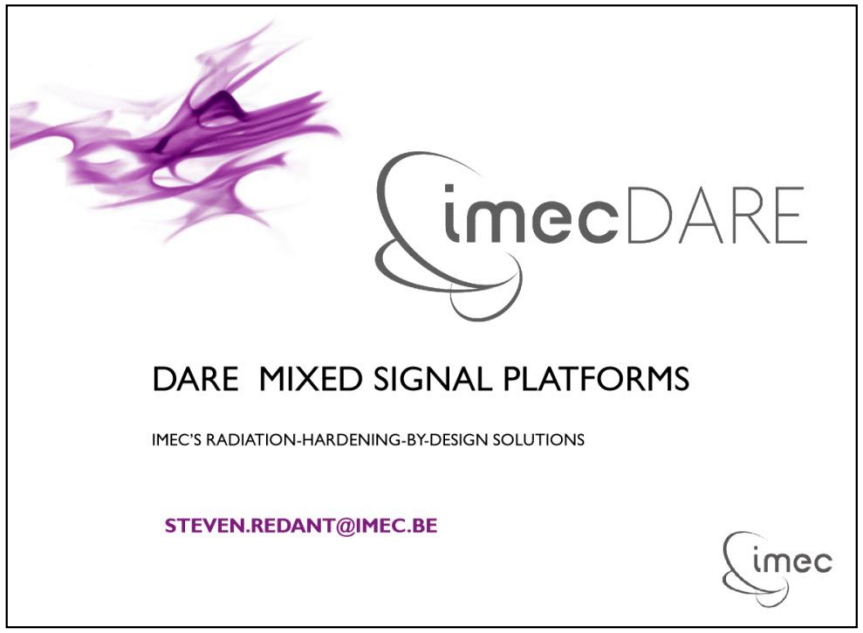
- Slides missing.

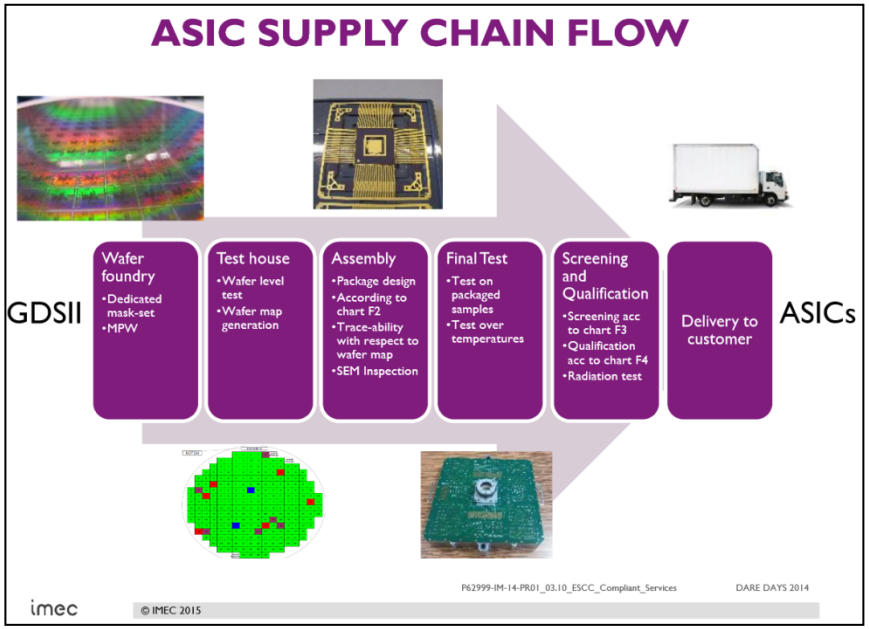
- Andrew Whitbeck of Fermi presented
- Automatic chip testing robot
- Used GLIB with GBT protocol for test
- Running VTRX links
- Radiation and thermal cycling to accelerate lifetime





- GLBD 5Gbps chip exists, available for use
- GBLD 10 Gbps in testing
  - Could be available soon-ish





- Commercial company in Belgium.
- Private research group.
- High end electronics research for multiple fields.
- Didn't really talk about rad-hard solutions.
- Selling access to private ASIC design library.
- Full ASIC design -> delivery (or steps thereof).

GBTx side discussions

- Pedro Leiato is good POC for GBTx software/firmware interface issues
- Schematic of GBTx on a board
  - https://www.ohwr.org/projects/gefe
  - Also look up Stand Alone Test Board from TWEPP 2014
- GBT-FPGA has transceiver setting to improve optical link quality (do a search for vdd control and pre-emphasis tap to find the file)
- Lecroy serial data analyser can see GBTx output. Don't probe on the board with the GBTx chip or you will see pre-emphasis spike. Need to use optical link to get off the board, then buy a SFP optical to electrical board and connect the probe here.

GBTx side discussions, cont.

- Internal Control interface example written by Pedro.
- Need to modify User Logic, GBT Example and Pattern Gen to take input from SC-IC block.
- Need to write Python -> Ipbus -> memory and connect the SC-IC block to this.
- Need to write Virtex 6 code to instantiate RAM IP block for Ipbus to write to.
- Pedro has board and code to test everything, may be good to determine failure details, but we would need to remove and re-bond the GBTx chip.
- **Can’t config high speed data link over SC -> must use fused chip if we don’t use I2C**