TWEPP-11

Topical Workshop on Electronics for Particle Physics

Vienna, Austria | 26-30 September 2011

The workshop will cover all aspects of electronics for particle physics experiments, and accelerator instrumentation of general interest to users (electronics for particle detection, triggering, data-acquisition systems, accelerator and beam instrumentation).

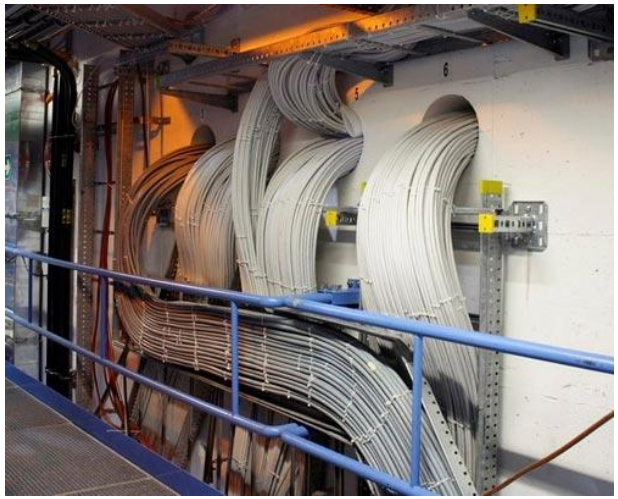
TWEPP HIGHLIGHTS

Peter W Phillips

Session Highlights:

POWERING

Recall: Powering the present SCT



- 4088 Detector Modules
- Independent Powering
  - 4088 cable chains
  - 22 PS racks
  - 4 crates / rack
  - (up to) 48 LV and 48 HV channels / crate
    - Installation a **major** logistical challenge!
- Overall efficiency ~40%
  - Cable R => voltage drops
  - Voltage limiter in line to protect against spikes due to sudden drops in load

ATLAS Strip Tracker Stavelets

or

A Tale of Two Stavelets

"It was the best of times, it was the worst of times, it was the age of wisdom, it was the age of foolishness, it was the epoch of belief, it was the epoch of incredulity, it was the season of Light, it was the season of Darkness, it was the spring of hope, it was the winter of despair..."

Peter W Phillips

STFC Rutherford Appleton Laboratory

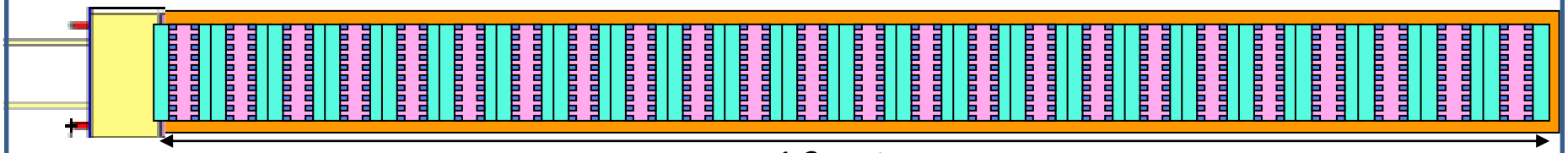
On behalf of

The ATLAS Strip Tracker Stavelet Community

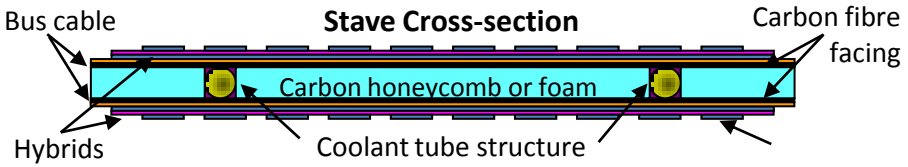
TWEPP, Vienna, September 26-30 2011

Science & Technology Facilities Council

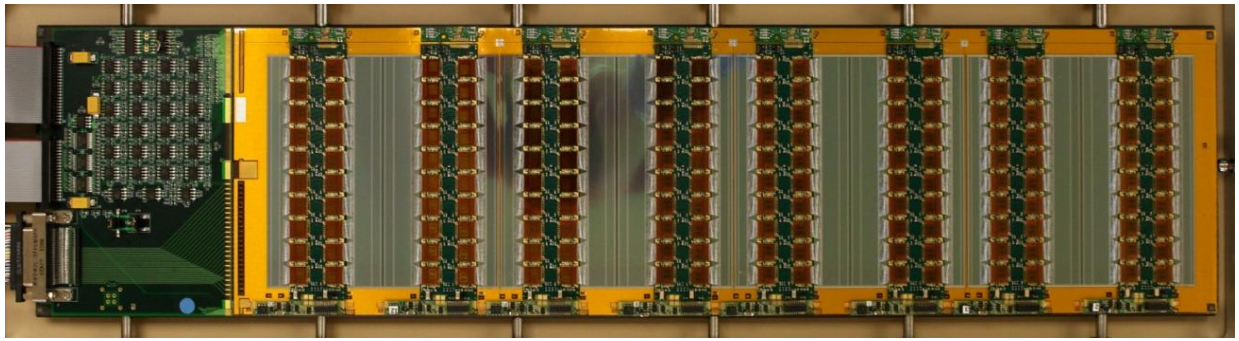
The Stave Concept



- Designed to reduce radiation length
  - Minimize material by shortening cooling path
  - Modules glued directly to a stave core with embedded pipes
- Designed for mass production
  - Simplified build procedure
  - Minimize specialist components
  - Minimize cost

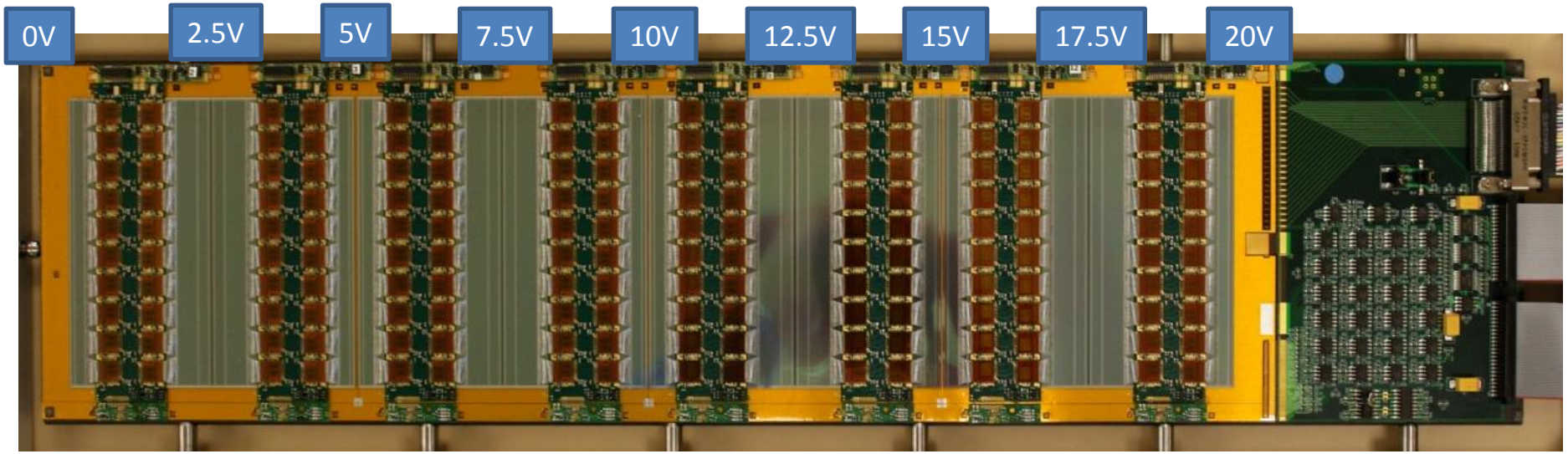


Stavelets



A Stavelet is a shortened stave prototype with up to four modules on each side. Results will be reported here for a Serially Powered Stavelet with four modules and a Stavelet with four modules fed by eight STV-10 DC-DC converters

Chain of Hybrids, individual shield pads



As first built, the current is routed between a module's two PPB boards by means of wirebonds and the bus tape, and the distributed shunt transistors are controlled by circuitry built into the hybrid. Separation of the sensor shield pads, with each hybrid either DC or AC coupled to its' sensor's shield, brought down the noise in comparison to the (common shield) results shown at TWEPP last year.

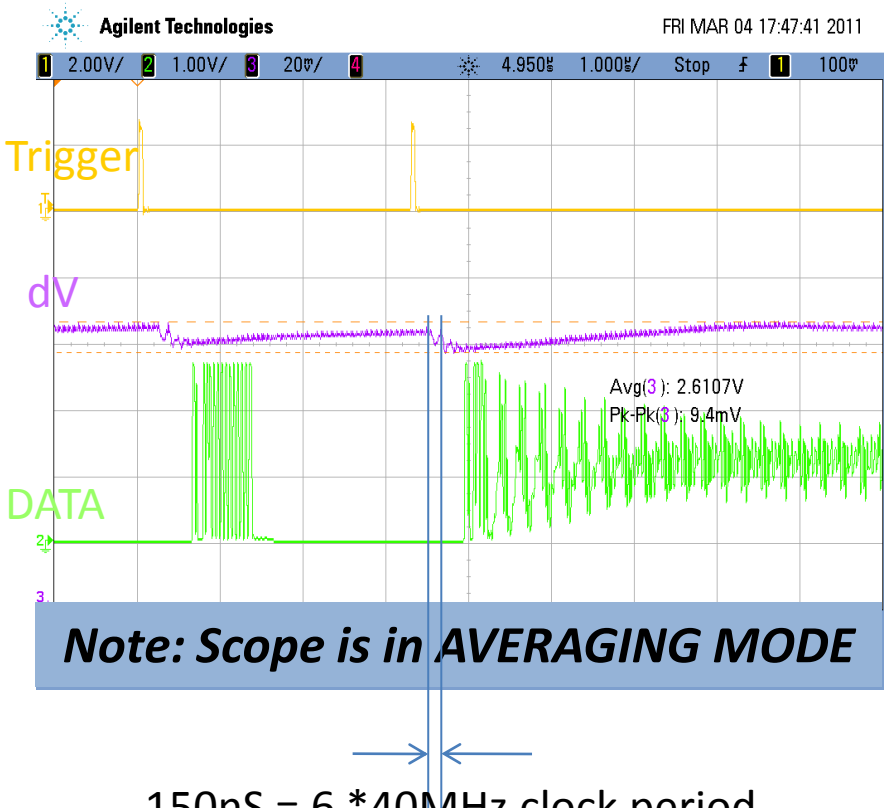
	H0		H1		H2		H3		H4		H5		H6		H7	
Column	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DC	DC	AC	**AC**	AC	AC	DC	DC	AC	AC	DC	DC	AC	AC	DC	DC
ENC	671	622	632	**678**	646	624	621	652	657	633	627	651	670	651	**619**	649

That looks OK: where's the catch?

Looking for signals correlated with readout: The Double Trigger Noise Test

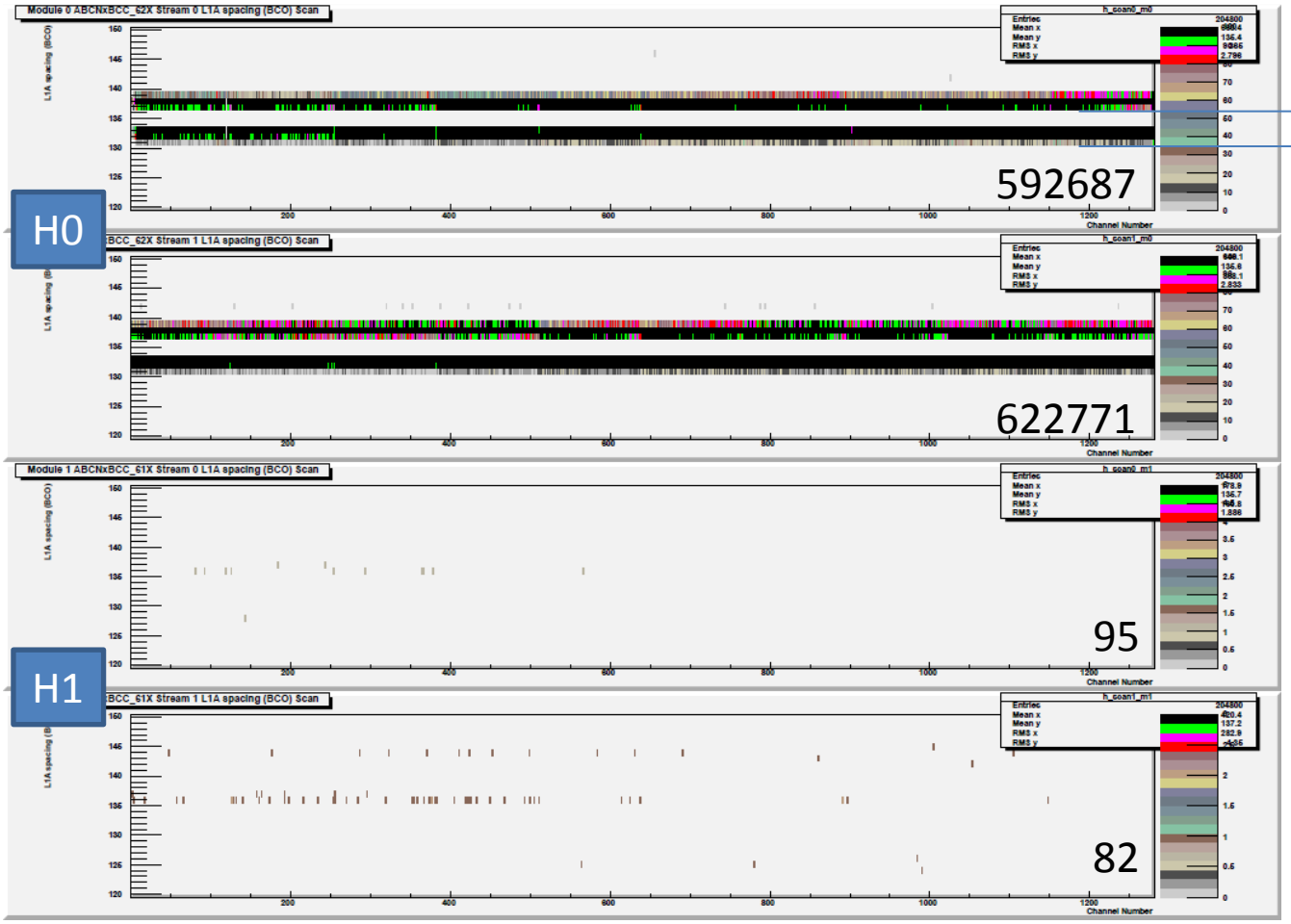
- The three point gain test used for ENC measurements uses optimistic trigger conditions
  - Cal pulse / trigger / readout / delay
  - Never more than one event in the pipeline
- In physics we would have random triggers, with many in the pipeline at once
  - Design a test to look for potential issues
- Send two triggers separated by a controlled, but variable number of clocks
  - Repeat for a series of fixed thresholds
  - Look for changes in occupancy
  - Look for voltage or current bumps correlated with the readout cycle
- With the ABCN25 chip, command reception triggers a surge in current
  - dV occurs between the power rails
  - This may inject signals into the front end

Custom Current Source @ 5A, HV 230V,
Two L1A separated by 134 BCO,
dV => diff probe between hybrid 0V & 2V5



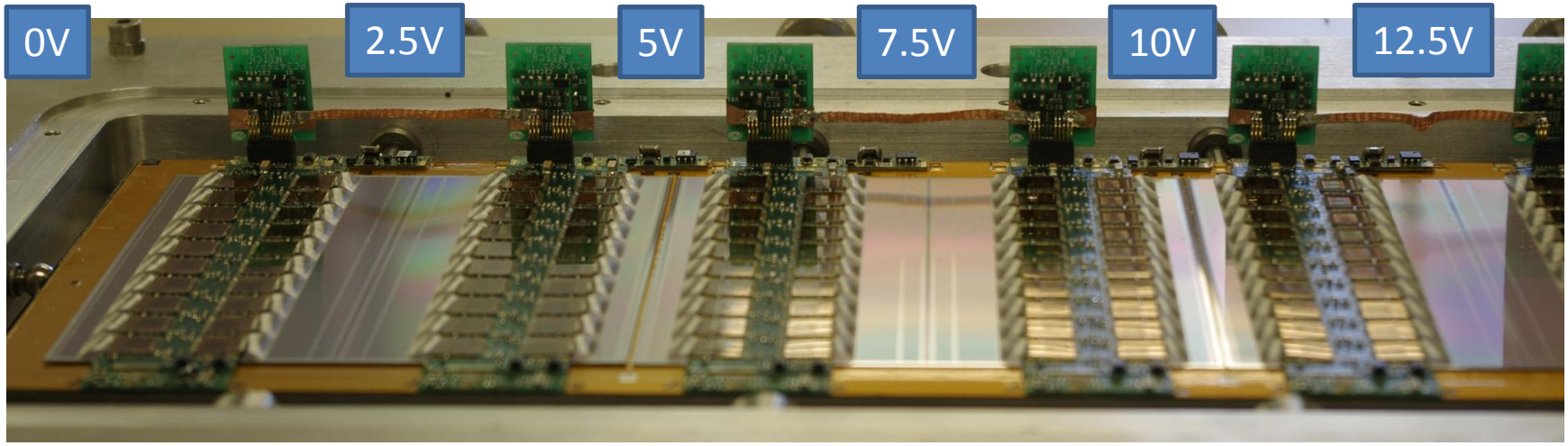
DTN Plots and a Very Basic Metric

Sum(hits): simply sum the number of hits shown in each double trigger plot



Stavelet M0 (H0/H1) DTN at 0.5fC

Chain of Hybrids with Coupled M-shunt Plugins

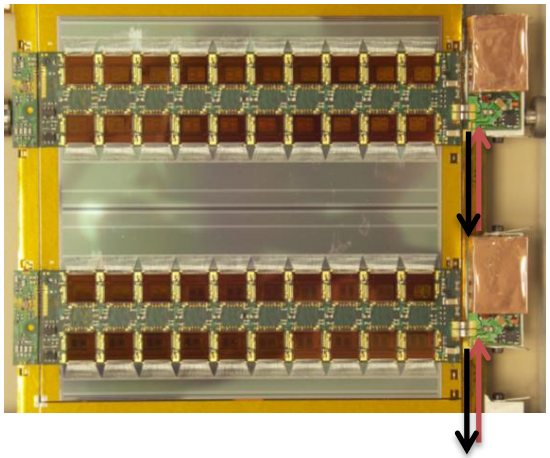


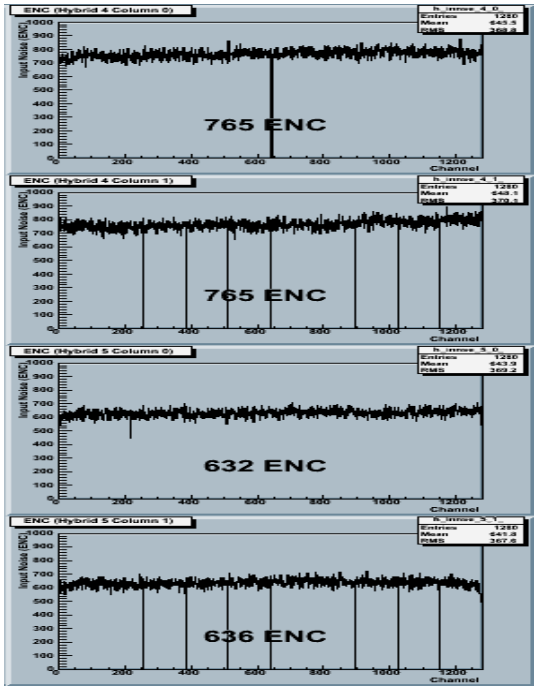
The bonds routing current between a module's two PPB boards have been pulled. Instead, the circuit is completed by copper braid. **Disconnection of the original route is of critical importance wrt DTN results.**

	H0		H1		H2		H3		H4		H5		H6		H7	
Column	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ENC	667	627	634	682	667	649	689	750	673	646	644	680	680	663	640	673
DTN @ 1.0fC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DTN @ 0.75fC	0	0													0	0
DTN @ 0.5fC	1085	582	6	62	429	329	79	586	298	359	28	76	554	565	29	158

Compared to original result, DTN is DOWN ☺ but ENC is UP ☹

DC-DC Stavelet Module (1)



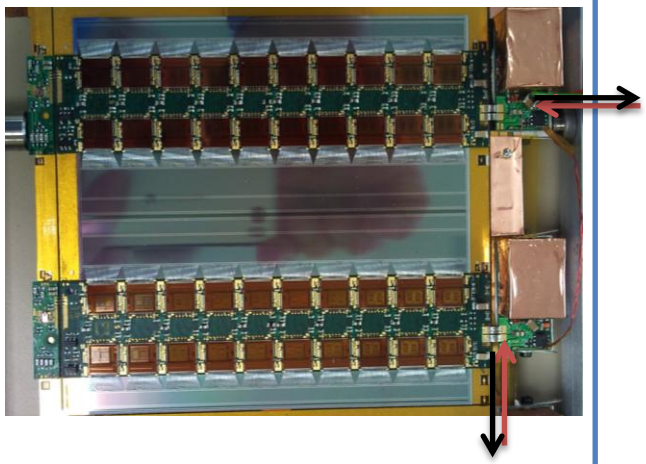


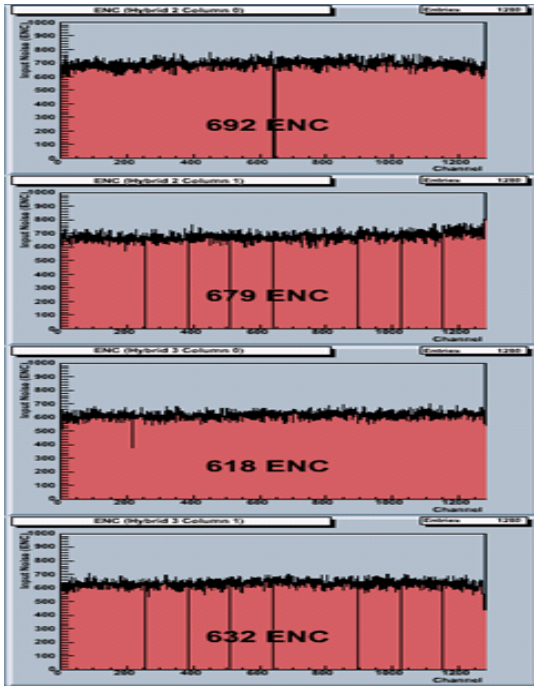
(1) Both converters powered from the bus

With both converters powered from the bus (1), the "upper" hybrid has ~120 ENC excess noise. Running each converter from a separate power feed (2) halves this excess to ~60 ENC.

In configuration (1) the power bus return trace provides a route between the two hybrid ground planes which runs parallel with the shield. Power currents flow through this trace (and hence the shield): increased noise is the result.

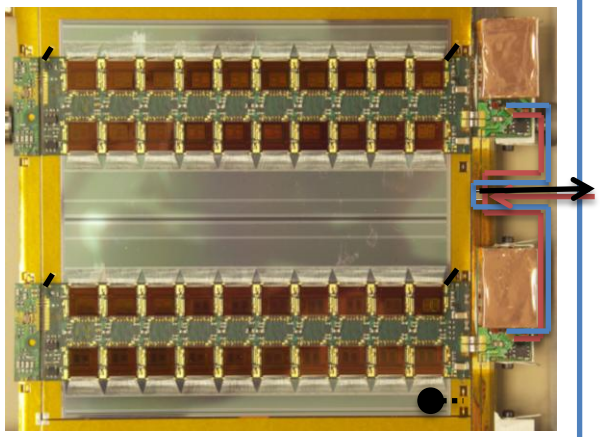
In configuration (2), separation of the power feeds has removed this possibility.

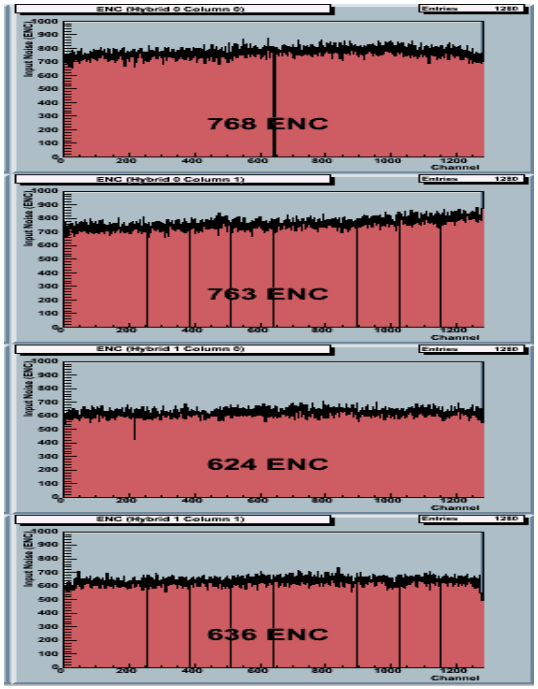




(2) Each converter powered from its own PSU

DC-DC Stavelet Module (2)



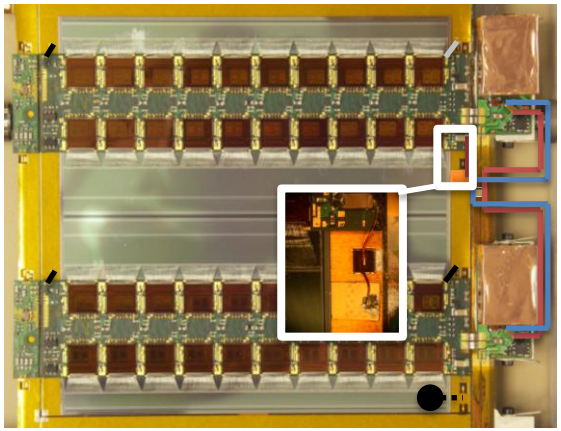


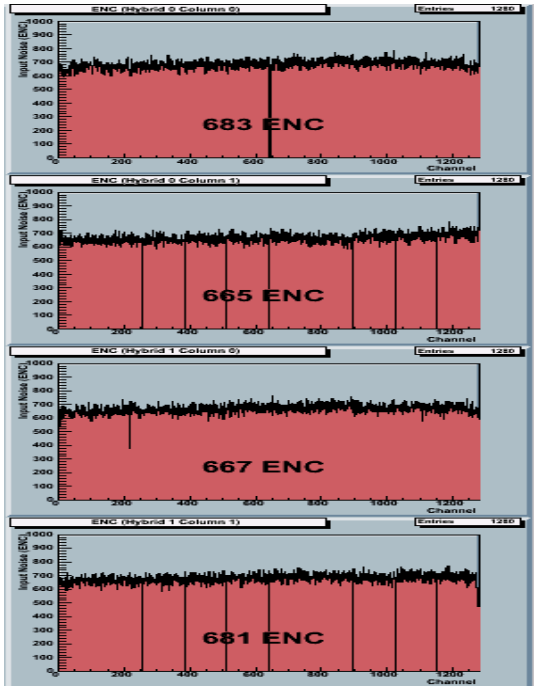
(3) ”STAR” configuration with Single backplane connection

Moving to the “STAR” configuration (3) yields results similar to the original one, however it should keep currents related to other modules out of the local loop.

Adding a second backplane connection (4) makes all the difference. Each hybrid now has its own HV bypass capacitor: the return path for signals originating in the “upper” hybrid need no longer involve the bypass cap of the “lower” hybrid. Both hybrids now have the same ~40 ENC excess noise.

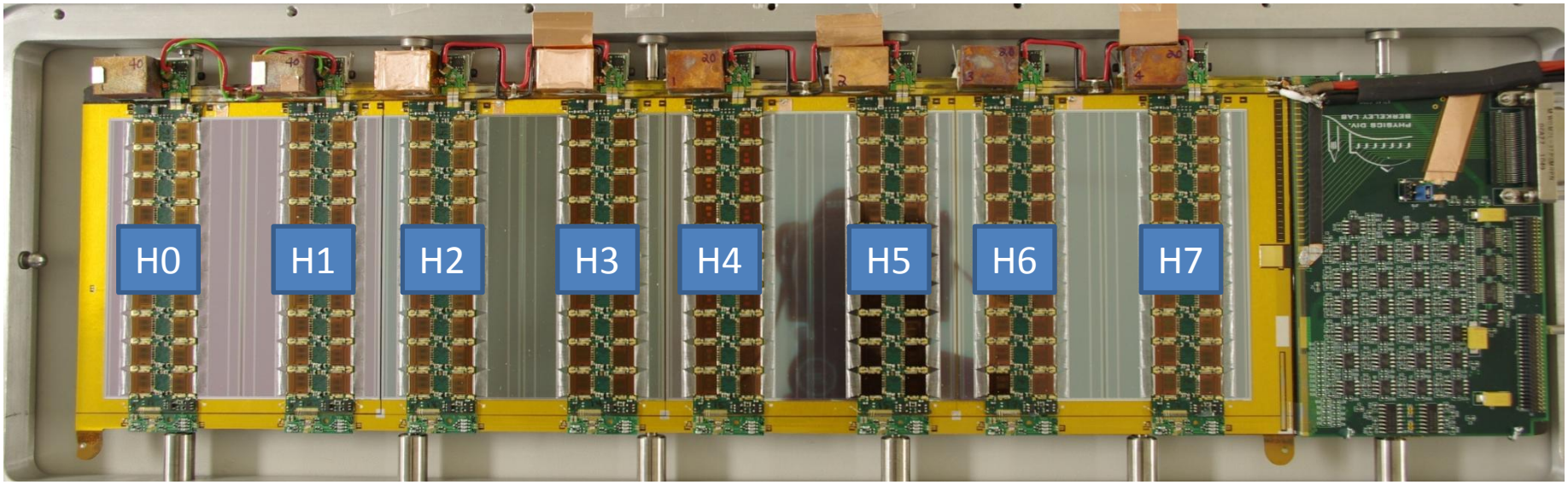
Proceed to mount further modules in configuration (4)!





(4) “STAR” configuration with Dual backplane connections

DC-DC Stavelet with Four Modules



Extra Noise compared to Reference Data

RAL 3PG @1fC - Liverpool Response Curve

Module	M0 (s/n M16)				M1 (s/n M13)				M2 (s/n M15)				M3 (s/n M17)				
Hybrid	H0		H1		H2		H3		H4		H5		H6		H7		
Column	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	
dENC	8	1	27	26	11	2	17	26	-10	-9	28	31	-26	-23	-2	-2	ENC
Shield	100 + Tape		100 + Tape		100 + Tape		100 + Tape		20		100		20		20		µm

DC-DC modules:

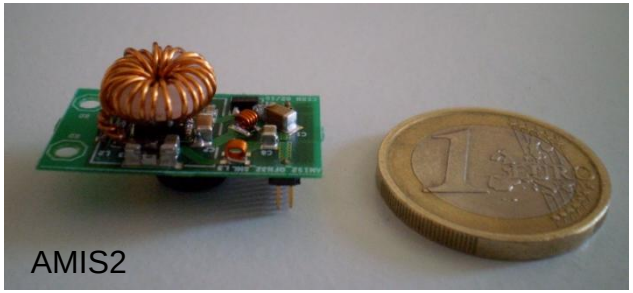
Gained experience
Material budget improvements
Grounding aspects

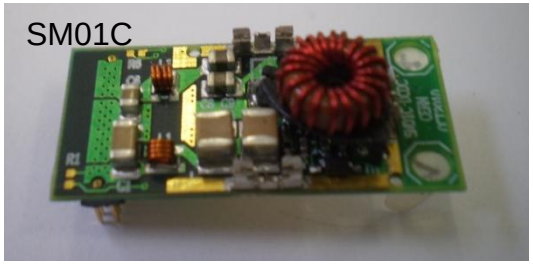
G. Blanchot, F. Faccio, S. Michelis

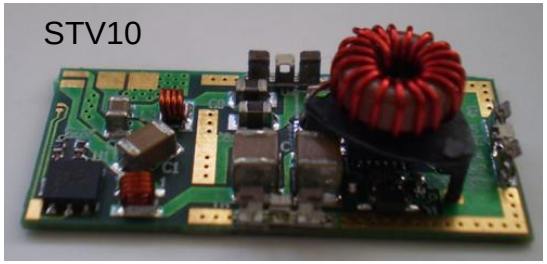
C. Fuentes, B. Allongue

The DCDC modules developed at CERN have been presented at TWEPP and at Power WG at several occasions:

- AMIS2 DCDC module:
  - Based on the AMIS2 ASIC, it delivers 3A at 2.5V.
  - Aimed for the powering HL-LHC front-ends with low power FE ASICs (in 130 nm).
  - It is a demonstrator for the low noise construction of a DC-DC converter module suitable for the LHC front-ends.
- SM01C module:
  - Based on the LTC3605 chip, it delivers up to 5A at 2.5V.
  - Aimed for the powering of HL-LHC front-end prototypes with currently available ASICs (>= 250 nm)
  - Same form factor and interface as for AMIS2.
  - Slightly higher noise than with the AMIS2 module.
- STV10 module:
  - Identical to SM01C, but is intended to be wire bonded on staves (no connector).
  - Mainly developed for the ATLAS stavelet.

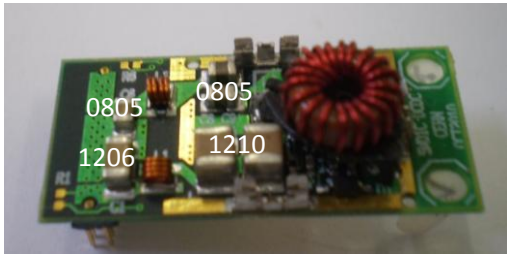

AMIS2

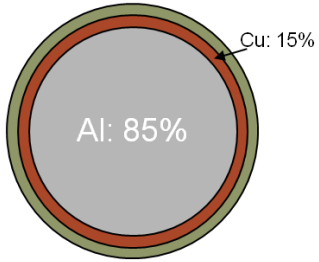

SM01C


STV10

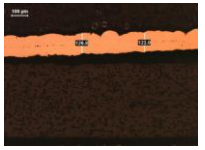
Mass Reduction Strategies

- Capacitors
  - 30% of the mass in the reference design of the DCDC module.
  - Large Caps 0.039% X0
  - Small Caps 0.016% X0
- Coil
  - Copper -> Enamelled Copper Clad Aluminium (ECCA)
    - 85% of aluminum core reduces the overall mass.
    - 15% of copper cladding helps in keep the resistance low.
  - At switch frequencies, all AC current flows in copper only due to skin effect.
  - DC current flows in Aluminum which has higher resistivity, increasing the losses
- Shield

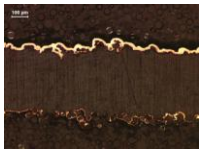




Construction	Attenuation	%X0
35 μm Cu foil box	36 dB	0.024
10 μm Cu on PE box	36 dB	0.0068
100 μm Al box	28 dB	0.0084



~100 μm

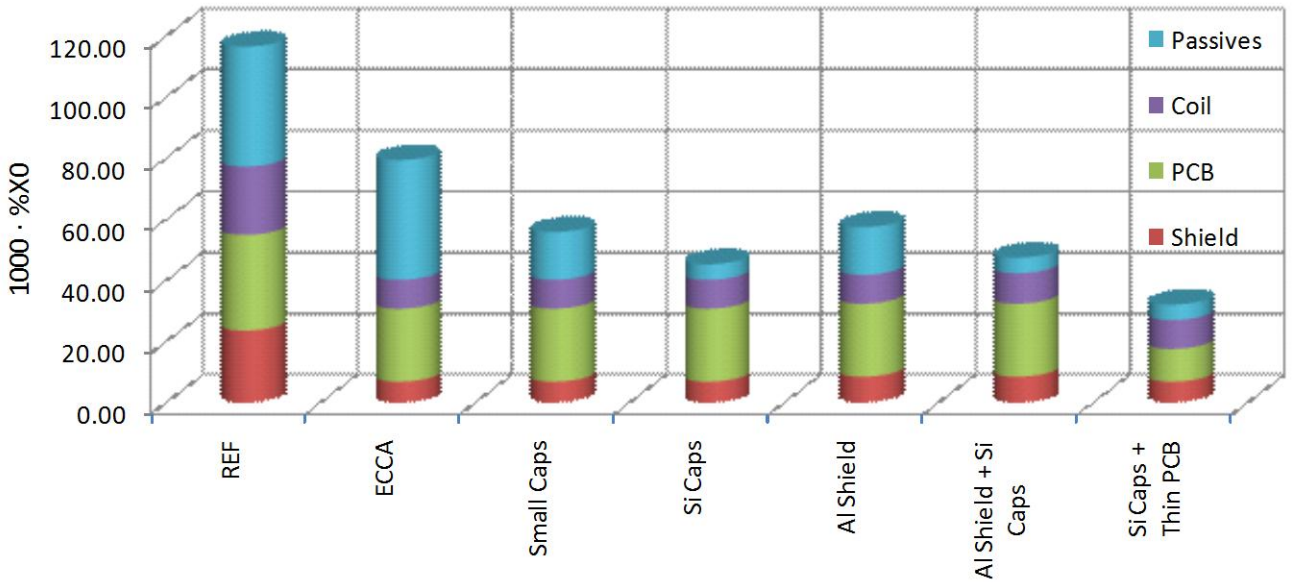


9–14 μm

Summarized from
G. Blanchot - TWEPP 2011 Power WG

Mass reduction strategies: summary

	REF	ECCA	Small Caps	Si Caps	Al Shield	Al Shield + Si Caps	Si Caps + Thin PCB
Reference	☑	☐	☐	☐	☐	☐	☐
ECCA inductor	☐	☑	☑	☑	☑	☑	☑
10µm coated shield	☐	☑	☑	☑	☐	☐	☑
Al foil shield	☐	☐	☐	☐	☑	☑	☐
Small capacitors	☐	☐	☑	☐	☐	☐	☐
Silicon capacitors	☐	☐	☐	☑	☐	☑	☑
300um thin PCB	☐	☑	☑	☑	☑	☑	☐
100um thin PCB	☐	☐	☐	☐	☐	☐	☑



DCDC modules based on a commercial chip are being tested with different systems.

- The converters are functional, deliver up to 5A, voltage is trimmed on demand, noise is low enough for most applications, can be turned on and off.
- Integration issues are rising up when using several converters to power large systems: common mode voltages, return paths, grounding configurations need optimization of the system.
- Results with the stavelet and with the supermodules, although this work is still in progress now, seem to show that noise levels close to those obtained with lab power supplies are in reach now.
- New prototypes based on the AMIS4 ASIC are now being tested.

DCDC modules can adapt for low mass systems

- The fraction of radiation length of the DCDC modules on the ATLAS stave can be divided by 4 with respect to the reference DCDC design.
- All the proposed mass reduction strategies are affordable, no exotic solution.
- Low mass DCDC converters represent a %X0 = 0.032, that if compared to the 0.53 of the modules themselves, is equivalent to 6% increase of mass only.

Grounding schemes

- Grounding schemes have a strong impact on the nosie performance observed by systems powered by DCDCs.
- Efforts must be focused now to get good noise performance of full systems: this is going to be explored on the stavelet and on the supermodule setups.

Session Highlights:

GROUNDING AND SHIELDING

EMC Issues in CMS Infrastructure

S. Lusin

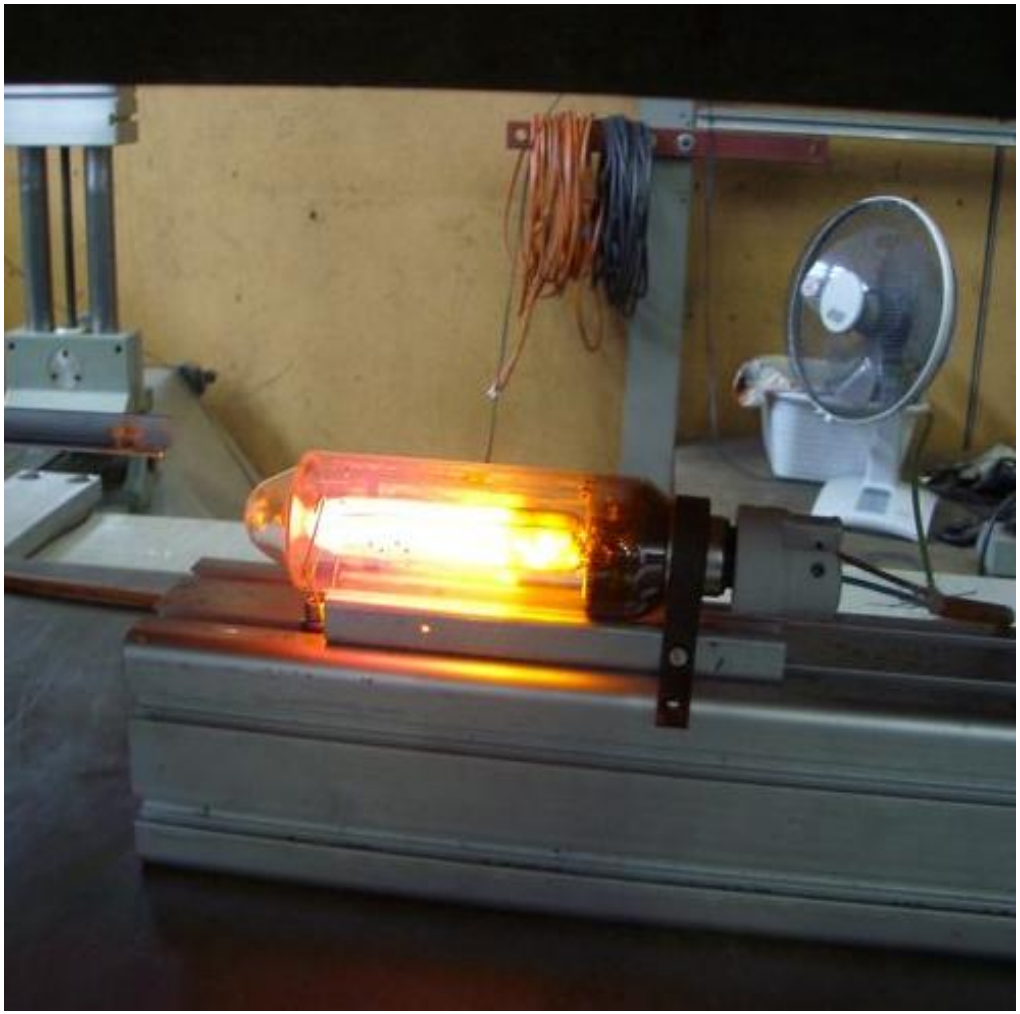
CERN

Services …

- **Very common to find detector-centric views during the design phase**
  - **Most coordination activities involve integration of subdetectors with one another**
- **Services are added as a parallel activity once global requirements become clearer**
  - **Services are "standard" in the sense that they use common industrial hardware**
  - **This common industrial hardware is then installed in an environment that is anything but standard**
- **Process of harmonizing detector subsystems with infrastructure is usually empirical and iterative**
  - **Typically initiated by the emergence of problems with detector operations**
    - Our awareness of these problems is not always immediate
  - **Could benefit from better anticipation of problems**

Lights …

- **Observed trigger rate bursts in CMS muon RPCs during cosmic-ray running**
  - Would last for minutes
  - Trigger rate of 1 kHz and above, nominal had been 200 Hz
- **Trigger rate bursts would begin when CMS magnetic field was turned on**
  - Only small group of chambers was affected
  - Affected chambers were in same area
- **Trigger rate bursts traced to mercury-vapor projector lights that had become unstable in the magnetic field**



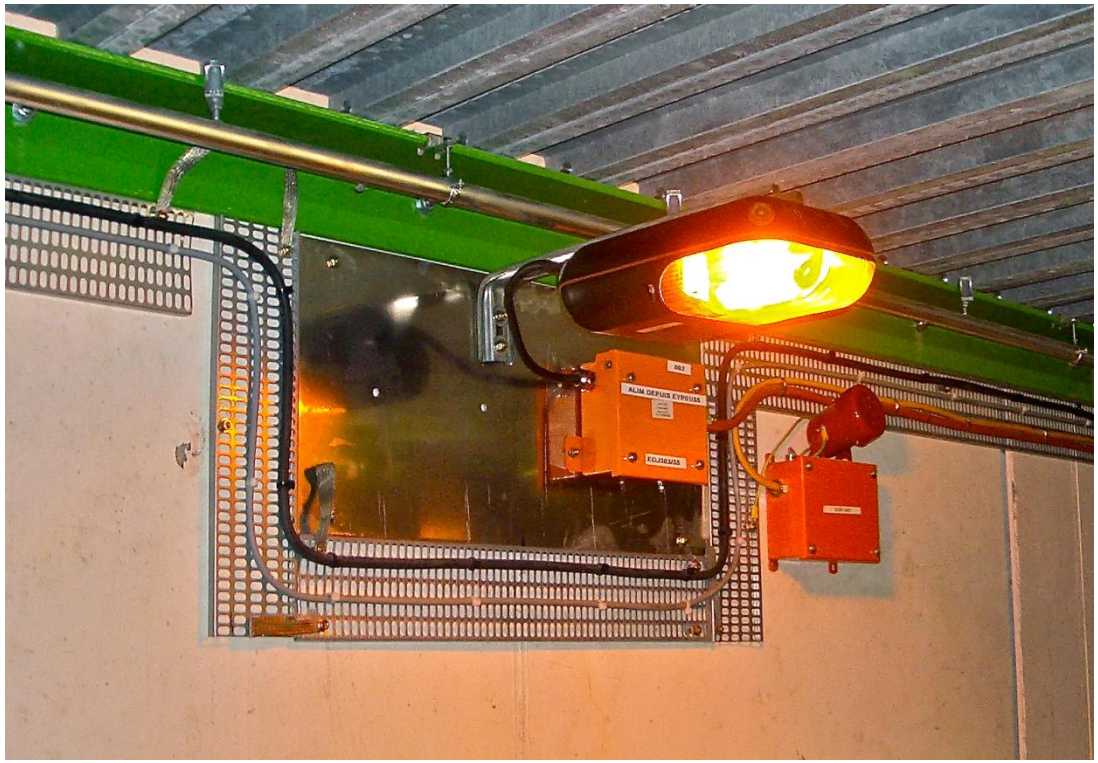
LPS lamp undergoing magnetic-field testing

Reorientation of LPS Lights

LPS lights in service galleries underneath the CMS detector were also unstable & flickering

- **These are safety lights. Turning them off is not an option.**
- **Results of testing showed that selective orientation could provide stable operation up to 1.2 KG**

Reorienting the tube axes parallel to the magnetic field resolved instability problem completely



Reoriented LPS light in CMS X0 zone in stable operation in magnetic field

Session Highlights:

TUTORIAL

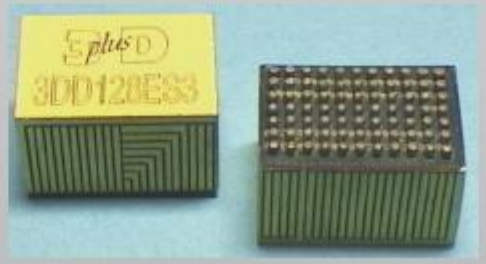
IC PACKAGING & INTERCONNECTION

Electronics Workshop - CERN

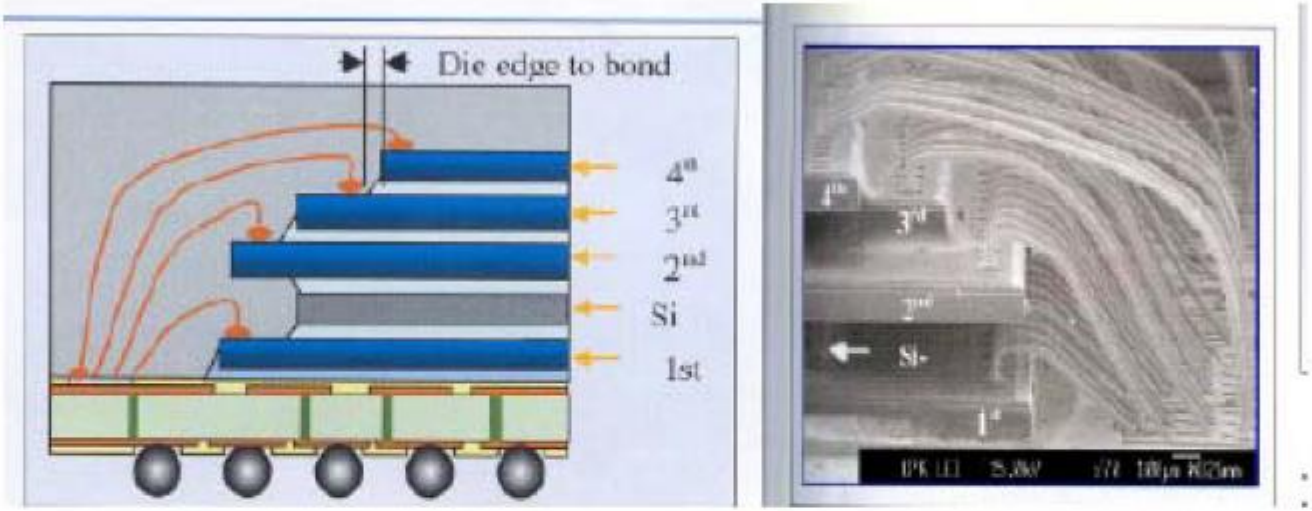
30th September 2011, Vienna

Dr. Alexandre VAL
3D PLUS
408 Rue Hélène Boucher - 78530 BUC
E-mail : alexandre.val@3d-plus.com

- Materials for Electronic
- Interconnections
- Packaging (QFN, PoP)
- Humidity / Hermeticity
- Wireless Interconnection
- 3D Packaging
- Conclusion



CHIP On CHIP - STATSChipPac



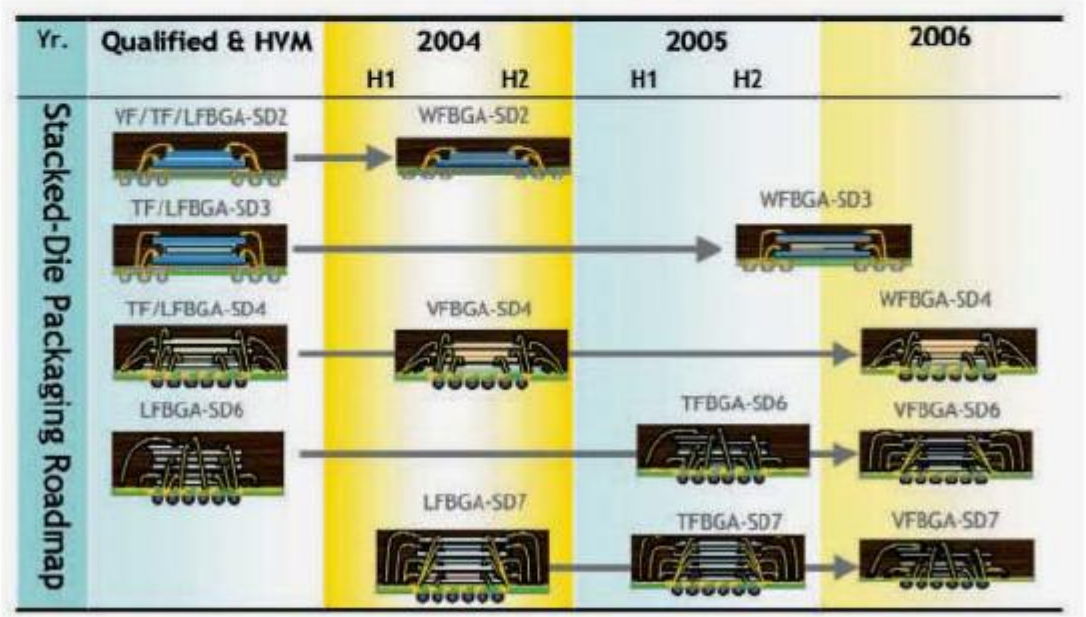
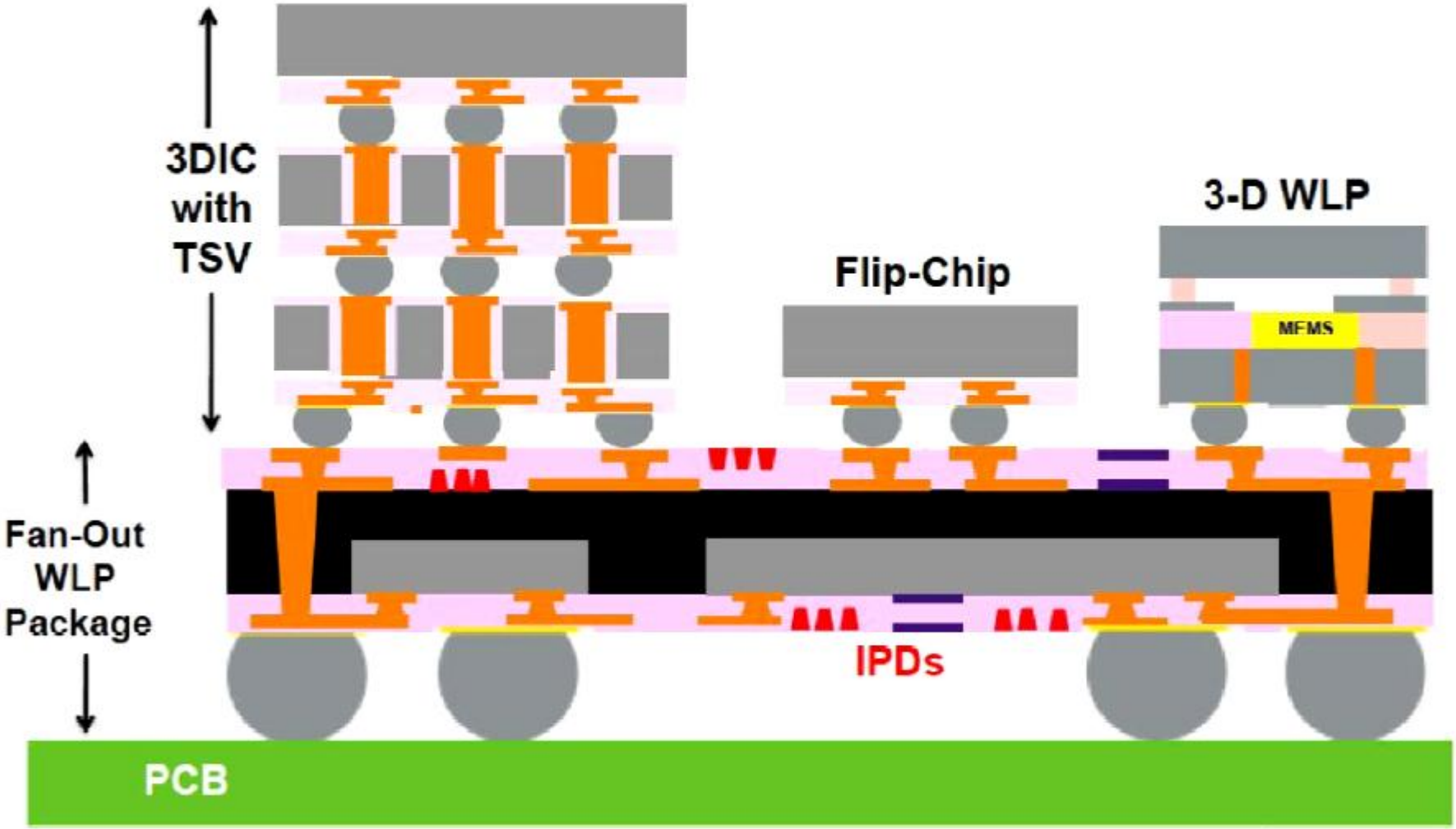


Figure 2. STATS ChipPAC's Stacked-Die Packaging Roadmap

Evolutions SiP & WLCSP

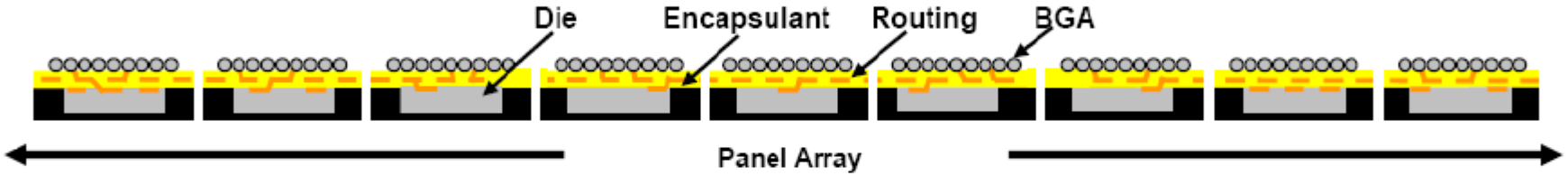


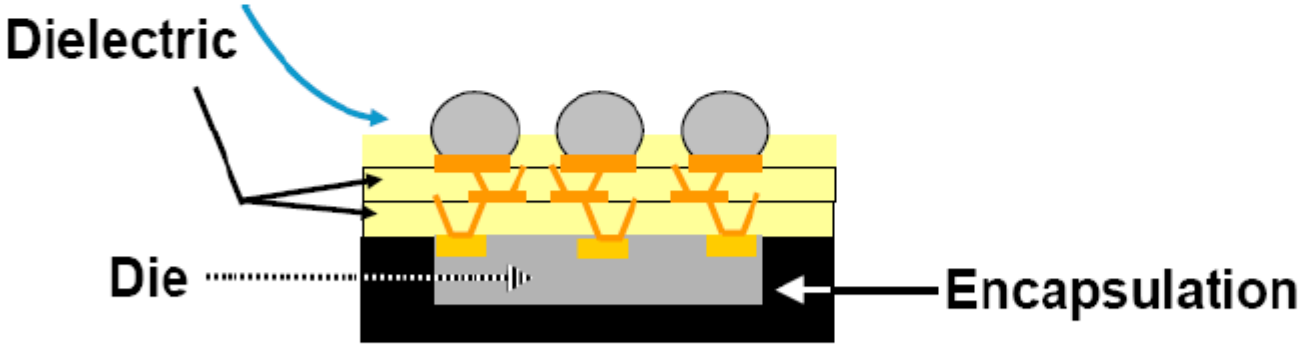
The solutions

FREESCALE RCP

"Redistributed Chip Package"

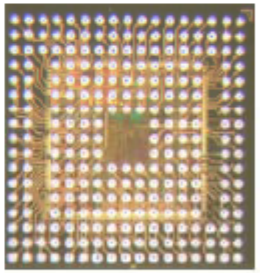
Freescale's RCP Packaging Technology





Freescale Produced *RCP*

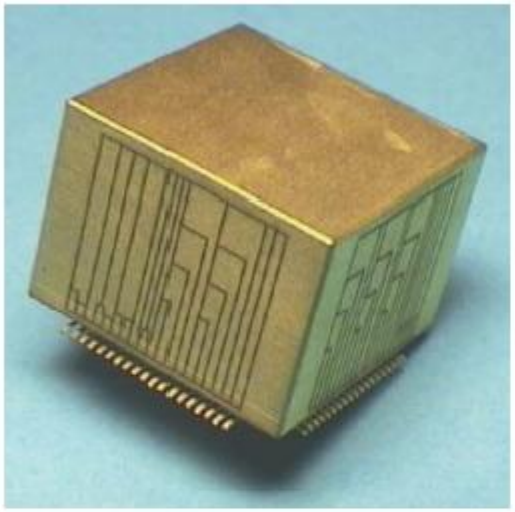
(BGA Bottom View)



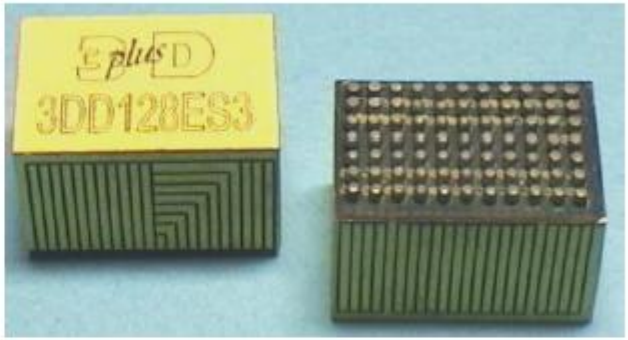
9 x 9-mm
280-I/O

Blocs « 3 D »

Applications

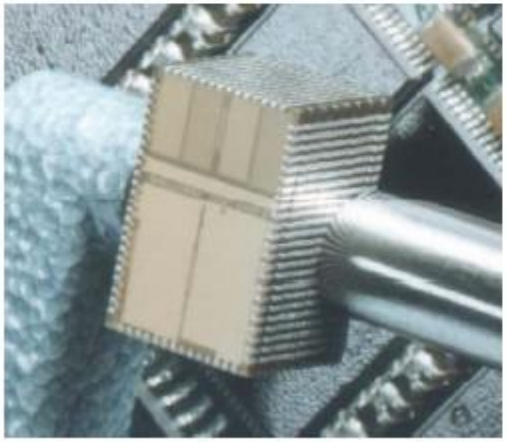


Module 3D with leads
(3D Plus)



Modules 3D BGA
(3D Plus)

Camera 3D
(3D Plus)



Memory modules 3D
(Shell Case)

MCM-Si stack 3D
(Leti)

Session Highlights:

SOCIAL

Official Conference Dinner Photograph (28/09/2011)

JAZZLAND

Joris Dudli “Sextett” feat. Anthony Wonsey (28/09/2011)