UNIVERSITY OF LIVERPOOL

Status and trends of silicon detectors for collider physics

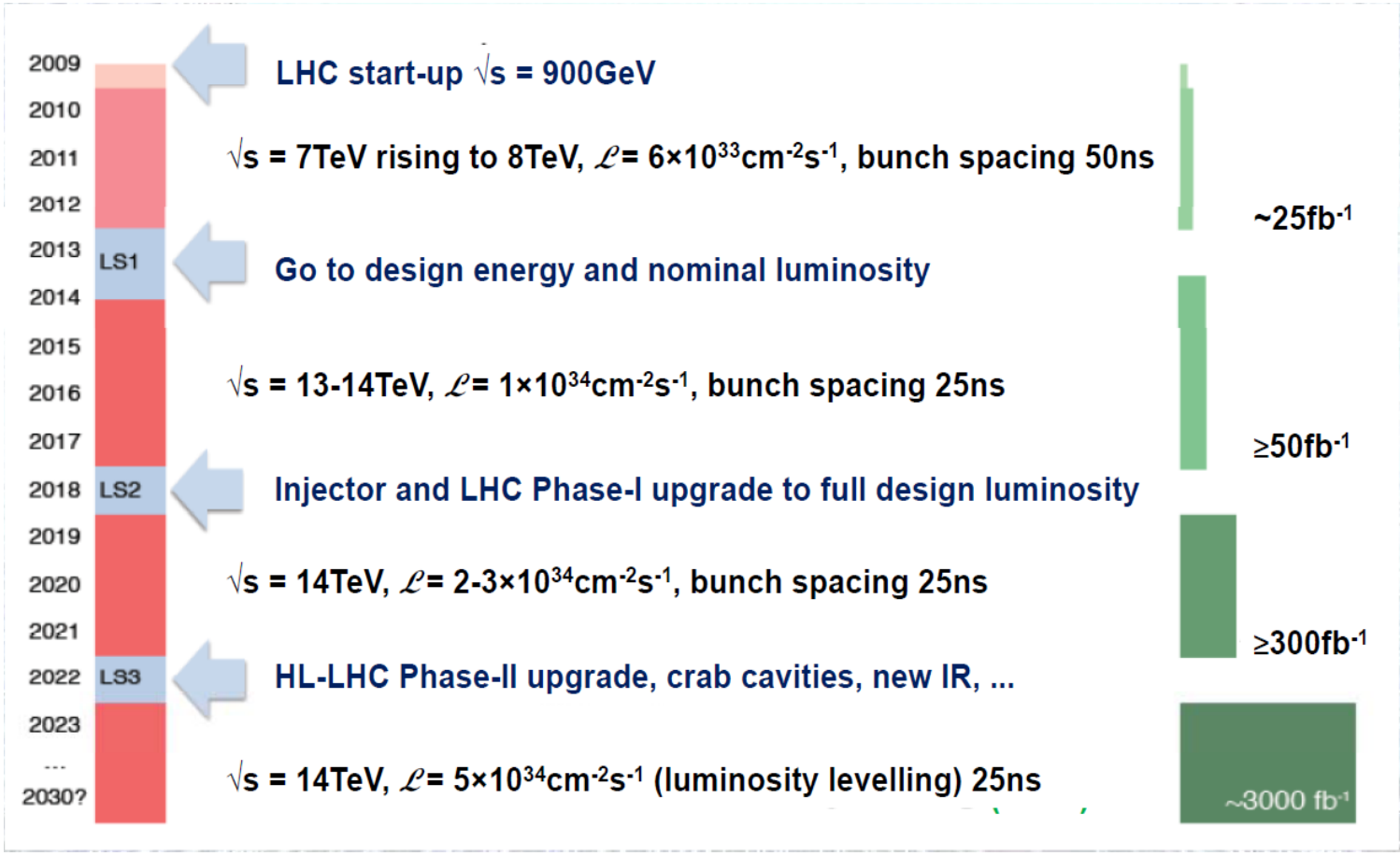
G. Casse

Outline

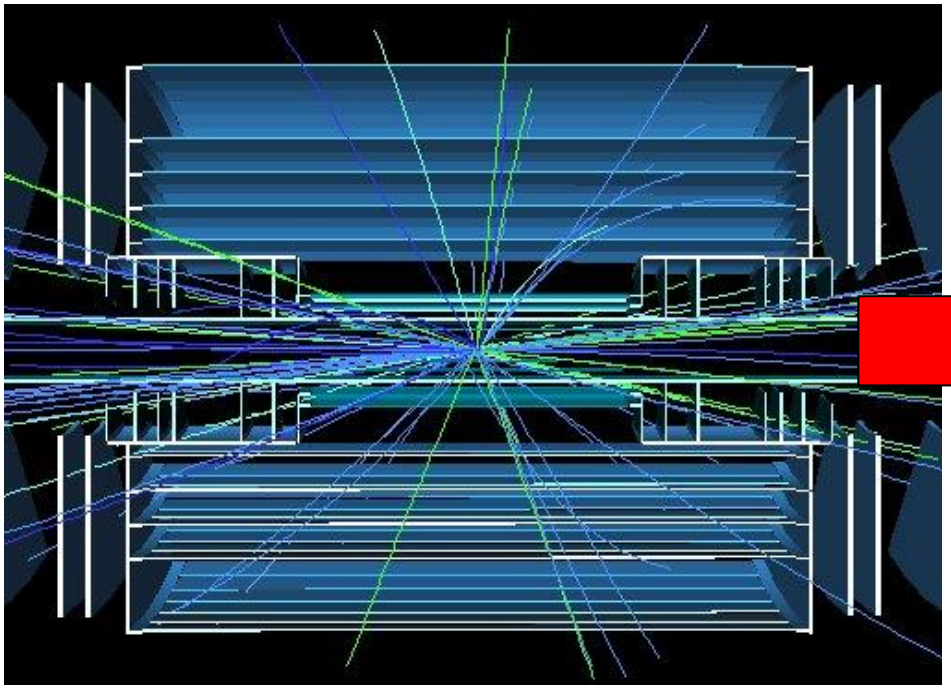
Silicon detectors are the devices of choice for vertex and tracker systems in high energy and (increasingly) nuclear physics experiments. This is due to their speed, low mass, relatively low cost and their surprising radiation tolerance. These characteristics have evolved over several order of magnitude since the introduction of segmented silicon sensors for tracking in the 1980' in CERN experiments. Their evolution is not slowing down. A review of the state-of-the-art and of current trends is given.

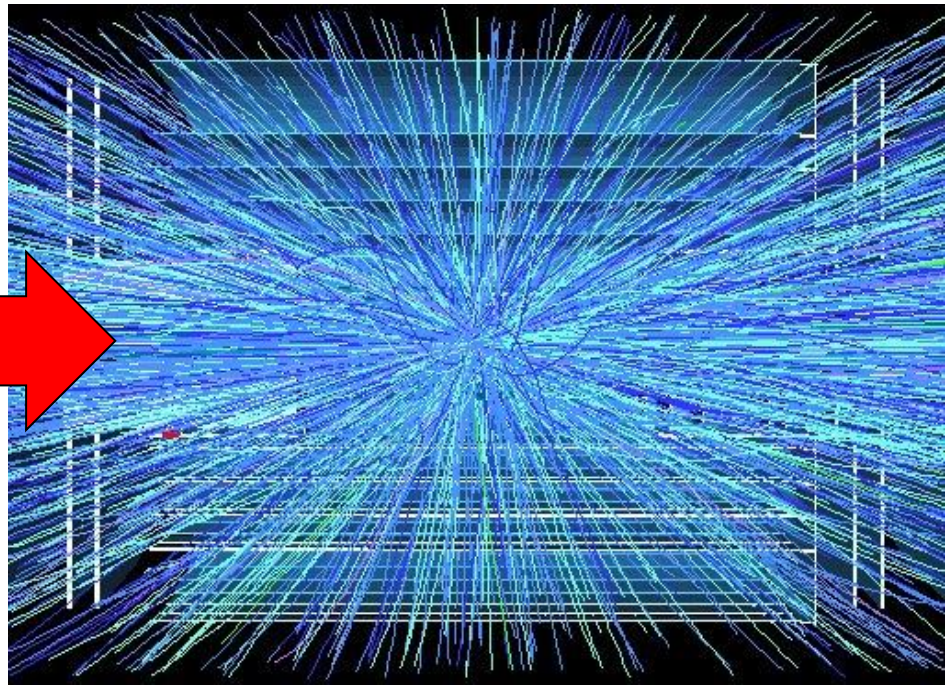
- Requirements for detectors for future hadron supercolliders
- Definition of the challenges: speed and radiation hardness
- Status
- Other future colliders
- Vertex and tracker sensors common requirements
- Summary

Possible 20 Year LHC Schedule



Radiation Background Simulation





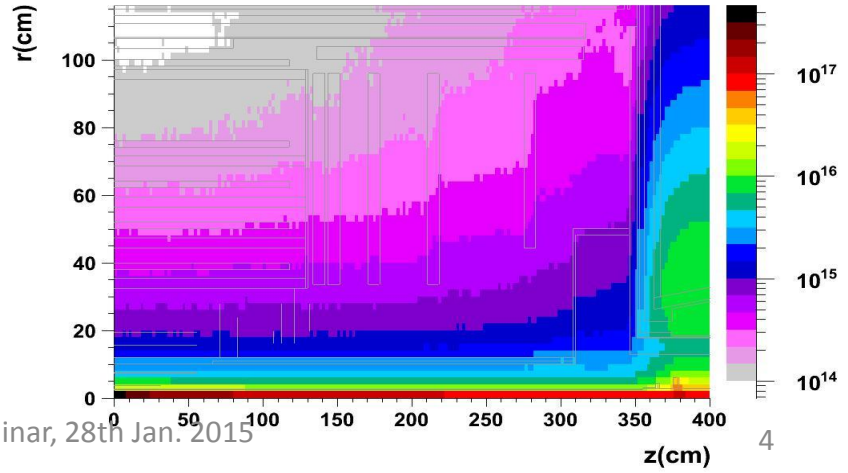
1 MeV neutron eq fluence

At inner pixel radii - target survival to 2-3×10^{16} n_{eq}/cm^2

Numbers obtained 9/10/09 (corresponding to new layout) assuming 3000fb-1 and 84.5mb

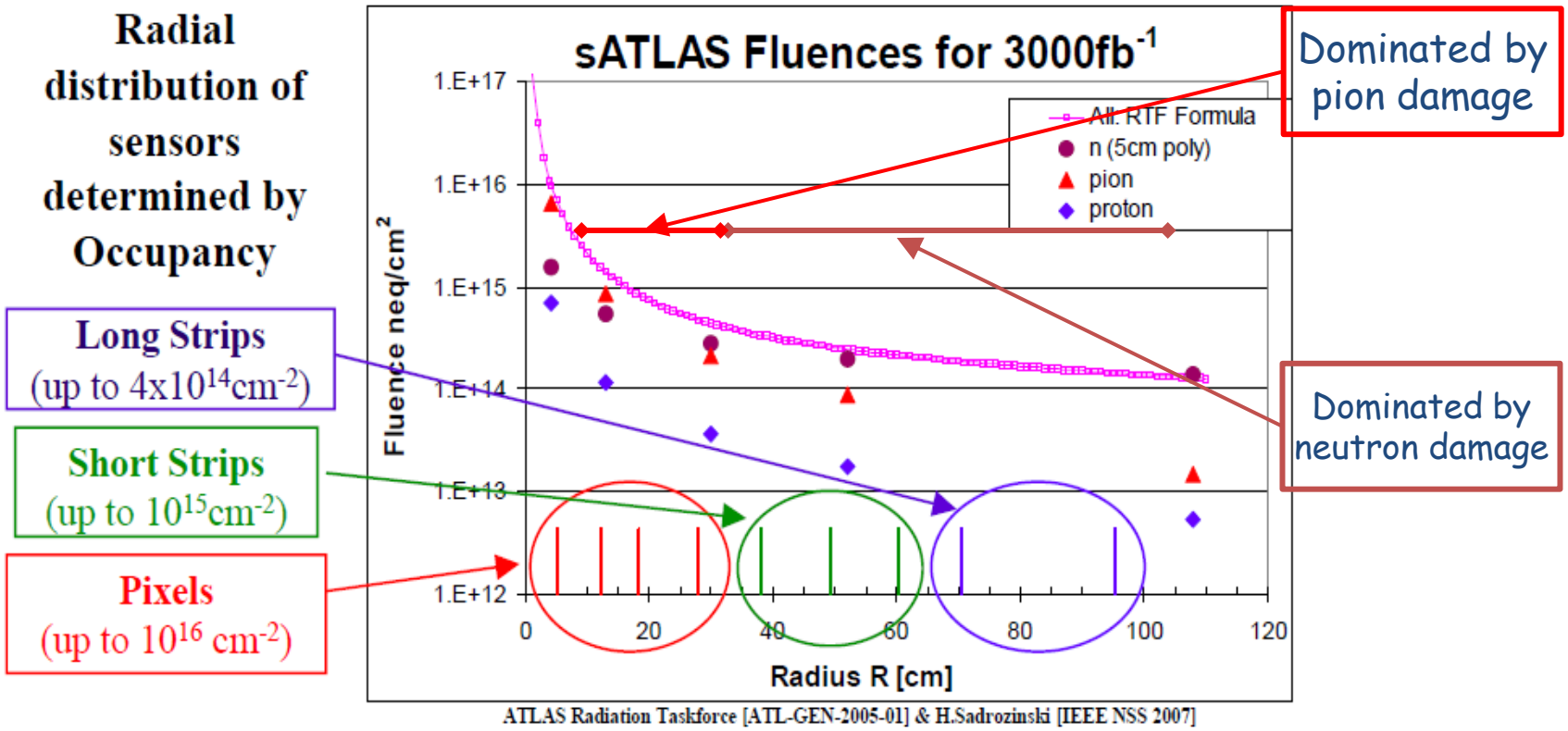
Strip barrel 1 (SS)	(r=38cm; z=0cm)	4.4x10^14
	(r=38cm; z=117cm)	4.9x10^14
Strip barrel 4 (LS)	(r=74.3cm; z=0.0cm)	1.6x10^14
	(r=74.3cm; z=117cm)	1.8x10^14
Strip Disc 1 (z=137.1, Rinner=33.6)		6.0x10^14
Strip Disc 2 (z=147.6, Rinner=33.6)		6.2x10^14
Strip Disc 3 (z=174.4, Rinner=33.6)		5.8x10^14
Strip Disc 4 (z=214.1, Rinner=33.6)		6.1x10^14
Strip Disc 5 (z=279.1, Rinner=44.4)		5.8x10^14
Strip Disc 5 (z=279.1, Rinner=54.1)		4.4x10^14
Strip Disc 5 (z=279.1, Rinner=61.7)		3.9x10^14
new		
Strip Disc 5 (z=279.1, Rinner=73.6)		3.0x10^14
Strip Disc 5 (z=279.1, Rinner=84.9)		2.7x10^14

For strips 3000fb^{-1} ×2 implies survival required up to ~1.3×10^{15} n_{eq}/cm^2



I. Dawson et al.

Radiation levels expected with sLHC



- **Radiation hardness requirements (including safety factor of 2)**
  - **2×10^{16} n_{eq}/cm^2 for the innermost pixel layers**
  - **1×10^{15} n_{eq}/cm^2 for the innermost strip layers**

[M.Moll]

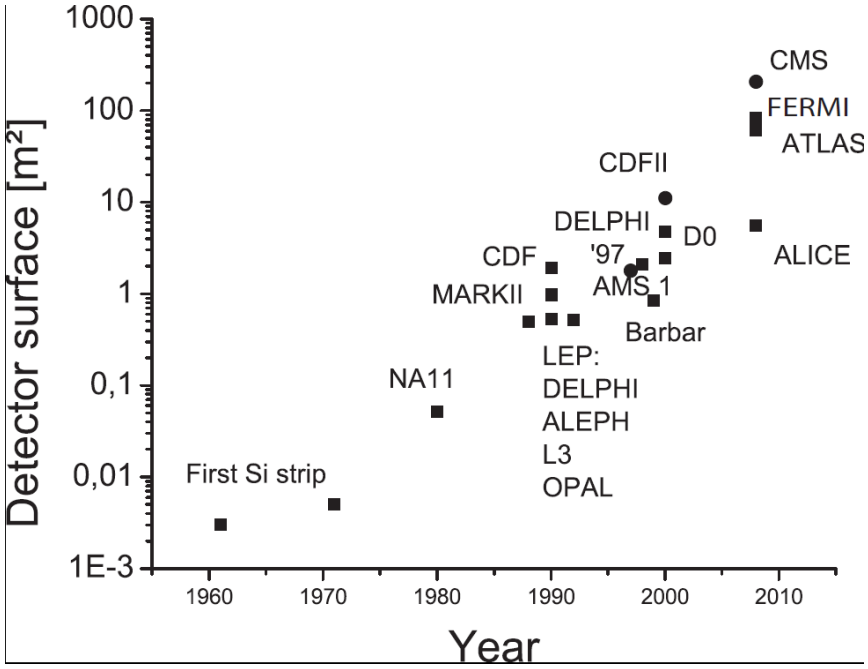
The rise of silicon detectors

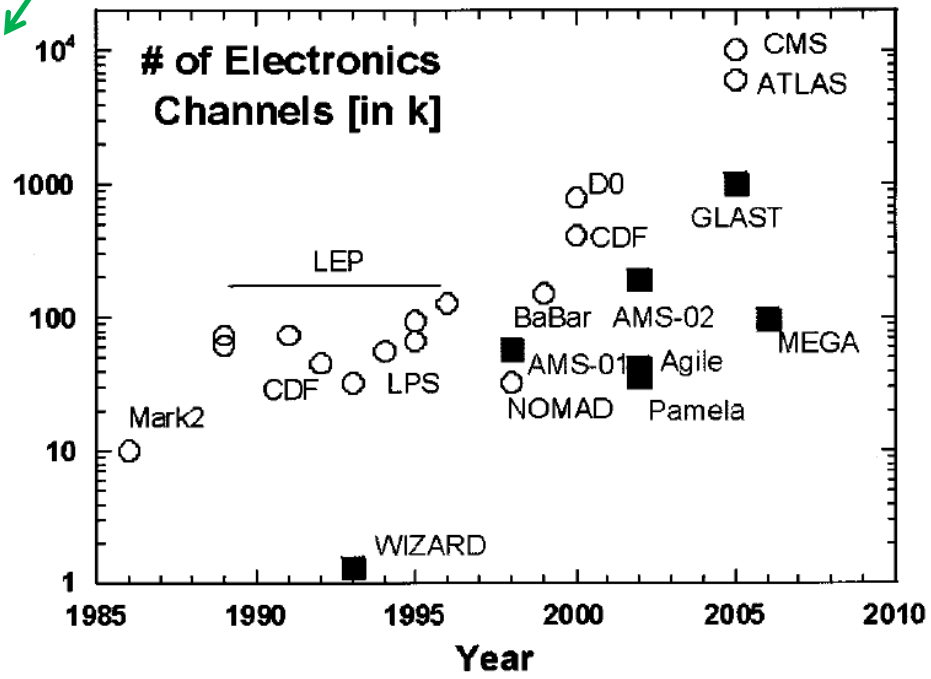
2022 (ish)

Up to by a factor of 10-40

Surface

# of channels





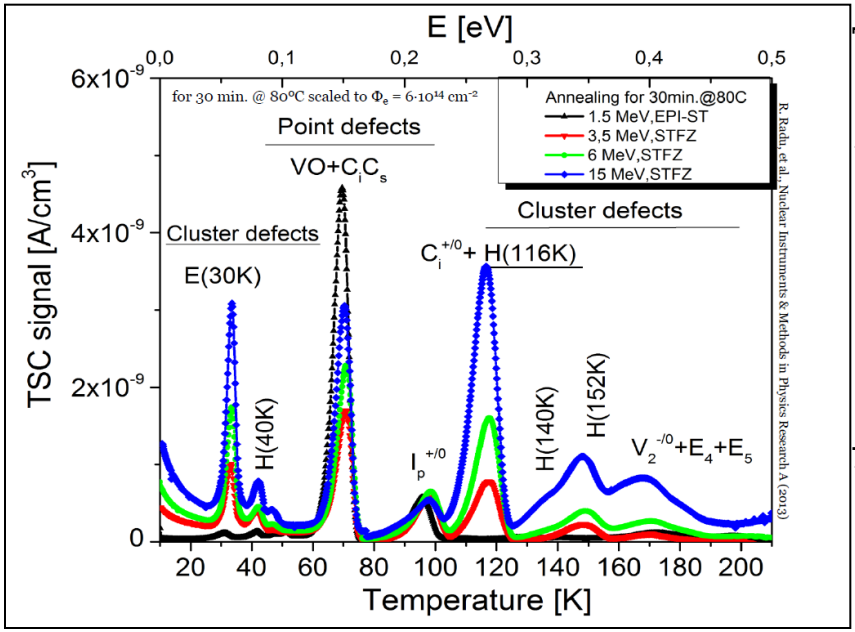
If surface is saturating, certainly the granularity is not.

Status of radiation hardness studies

- Crucial point for Vertex and Tracker sensors
- Silicon still the forefront runner, no serious possibility to change track within the timescale (possible exception, diamond for innermost layer....).
- Dedicated R&D activity within the upgrading experiments and a dedicated community (**CERN-RD50: http://rd50.web.cern.ch/rd50/**). Most advanced results from this community.

Defect Characterization

- Defect characterization
  - Aim:
    - Identify defects responsible for Trapping, Leakage Current, Change of N_{eff}, Change of E-Field
    - Understand if this knowledge can be used to mitigate radiation damage (e.g. defect engineering)
    - Deliver input for device simulations to predict detector performance under various conditions
  - Method: Defect Analysis on identical samples performed with various tools inside RD50:
    - **C-DLTS** (Capacitance Deep Level Transient Spectroscopy)
    - **I-DLTS** (Current Deep Level Transient Spectroscopy)
    - **TSC** (Thermally Stimulated Currents)
    - **PITS** (Photo Induced Transient Spectroscopy)
    - **FTIR** (Fourier Transform Infrared Spectroscopy)
    - **RL** (Recombination Lifetime Measurements)
    - **PC** (Photo Conductivity Measurements)
    - **EPR** (Electron Paramagnetic Resonance)
    - **TCT** (Transient Current Technique)
    - **CV/IV** (Capacitance/Current-Voltage Measurement)
  - RD50: several hundred samples irradiated with protons, neutrons, electrons and ^{60}Co-γ



[R.Radu, 22nd RD50 Workshop, 3-5 June

Example: TSC measurement on defects produced by electron irradiation (1.5 to 15 MeV)

… significant progress on identifying defects responsible for sensor degradation over last 5 years!

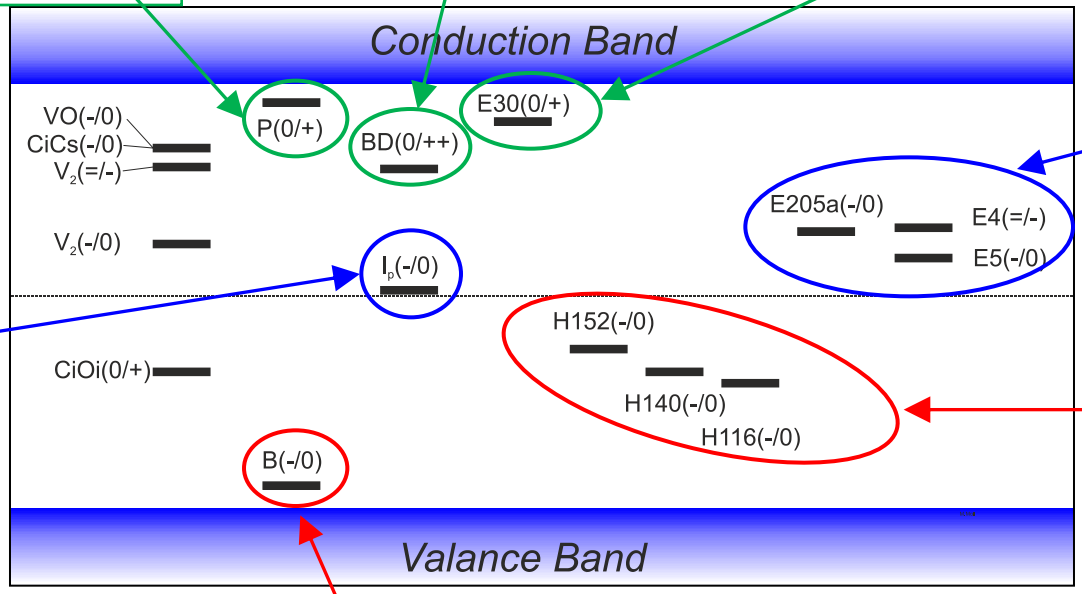
Summary on defects with strong impact on device performance after irradiation

- Some identified defects

Phosphorus: shallow dopant (positive charge)

positive charge (higher introduction after proton than after neutron irradiation, oxygen dependent)

positive charge (higher introduction after proton irradiation than after neutron irradiation)



Leakage current

E4/E5: V_3 (?)

leakage current & neg. charge

current after γ irrad, V_2O (?)

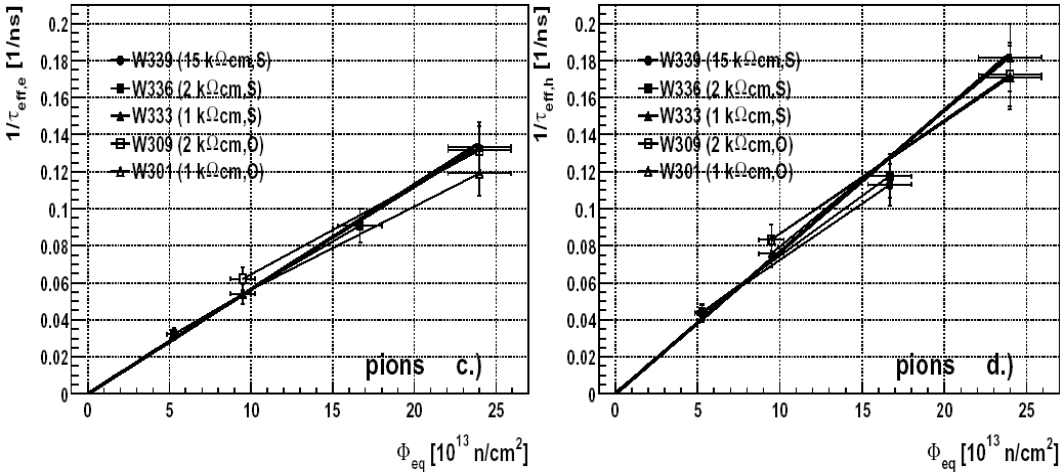
Reverse annealing (negative charge)

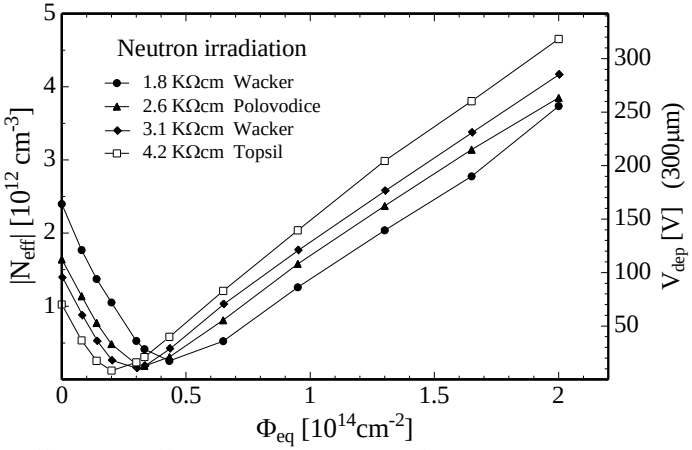
Boron: shallow dopant (negative charge)

A table with levels and cross sections is given in the next slide (spare slide).

- Trapping: Indications that E205a and H152K are important (further work needed)
- Converging on consistent set of defects observed after p, π, n, γ and e irradiation.
- Defect introduction rates are depending on particle type and particle energy and (for some) on material!

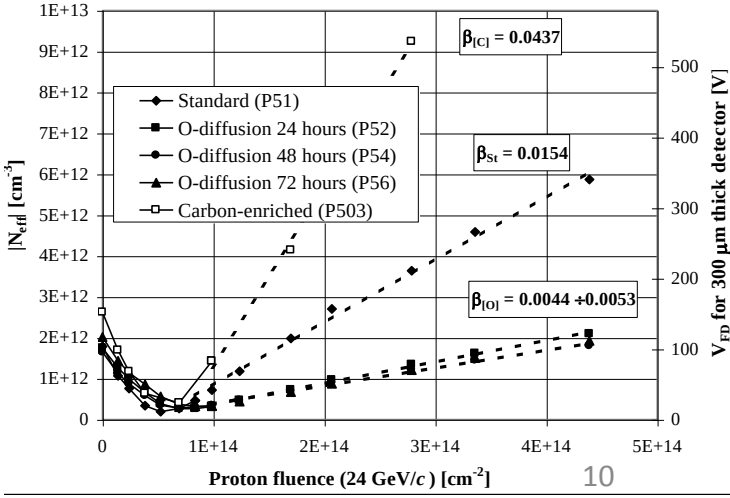
Radiation tolerance prediction: “old” method



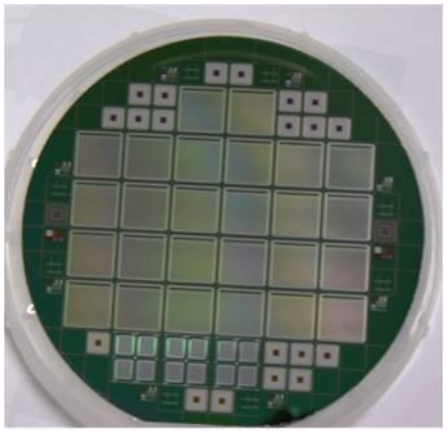


The Charge Correction Method (based on TCT) for determination of effective trapping times requires fully (over) depleted detector.

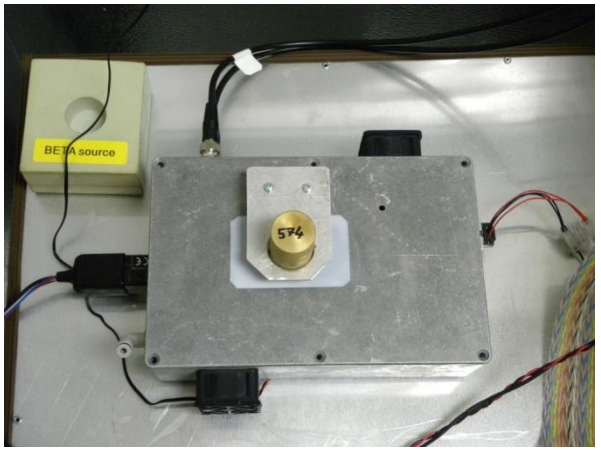
“Good” operation of sensors was based on the ability to provide a bias voltage corresponding to 120-130% of the full depletion voltage. But the VFD would be well over 10000V at HL-LHC doses ....

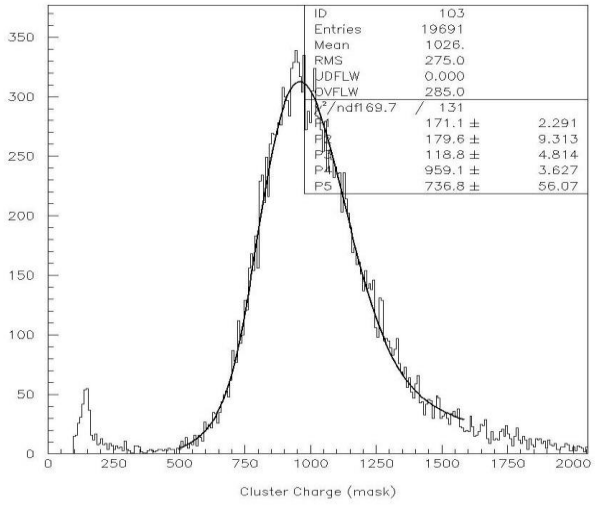


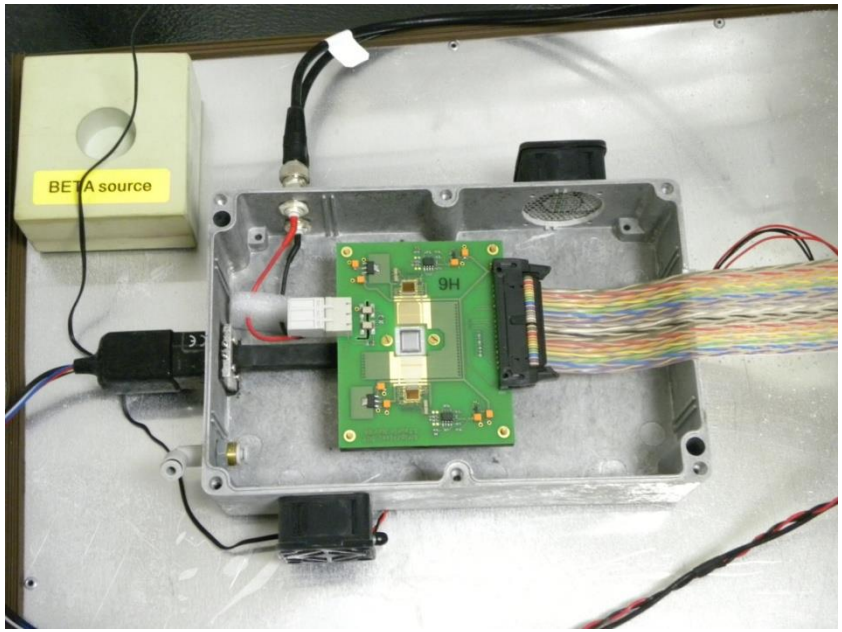
More relevant method: analogue readout with LHC speed electronics



Mip signal from ^{90}Sr source







Analogue information from the Alibava board (equipped with Beetle chip)

Irradiated silicon sensors

Low density of charge carrier in "non depleted" bulk, electric field at any voltage in the "neutral bulk", high level of trap concentration.

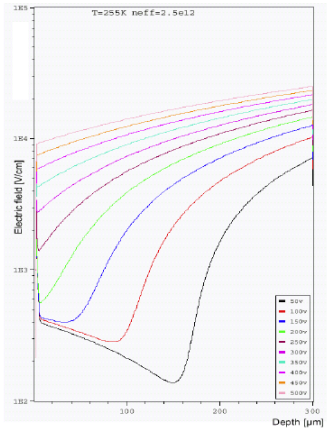
$$Q_{tc} \cong Q_0 \exp(-t_c/\tau_{tr}),\ 1/\tau_{tr} = \beta\Phi.$$

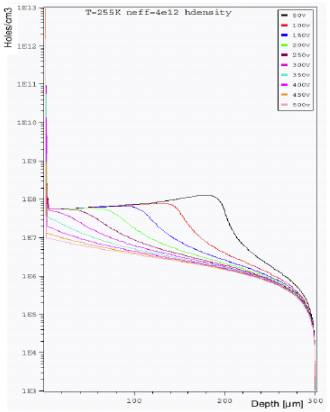
$\lambda_{Max,n}\ (\Phi=1e14) \cong 2400\mu m$

$\lambda_{Max,n}\ (\Phi=1e16) \cong 24\mu m$

$\lambda_{Max,p}\ (\Phi=1e14) \cong 1600\mu m$

$\lambda_{Max,p}\ (\Phi=1e16) \cong 16\mu m$





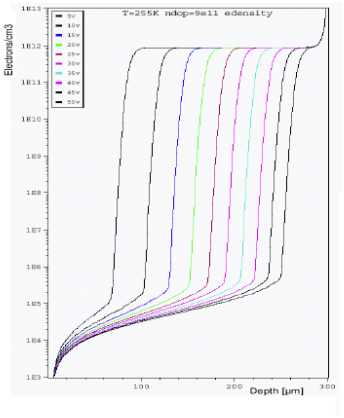


Fig. 19 Electric field profile and majority carrier concentration in an irradiated (4x1(cm^{-2}) silicon detector with the bias voltage as a parameter. V_{fd} is ~200V. Note the low de of free charge carrier (right) in the non-depleted bulk (after inversion depletion goes from left to rignt).

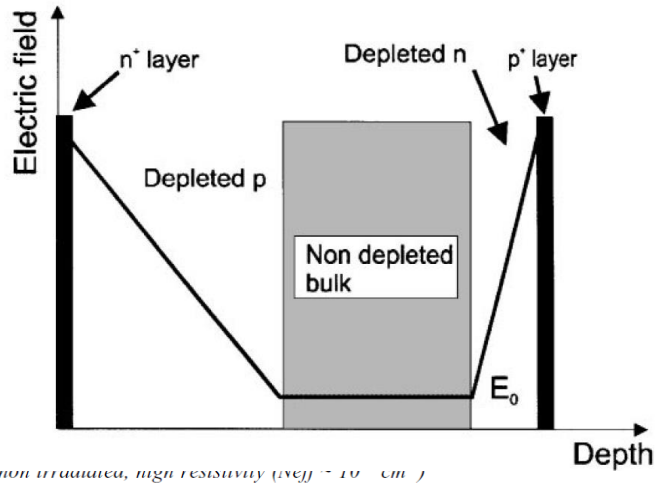


Fig. 20 Majority carrier concentration in a non irradiated, high resistivity (ve[illegible] n-type silicon detector with the bias voltage as a parameter. Depletion goes from left to right.

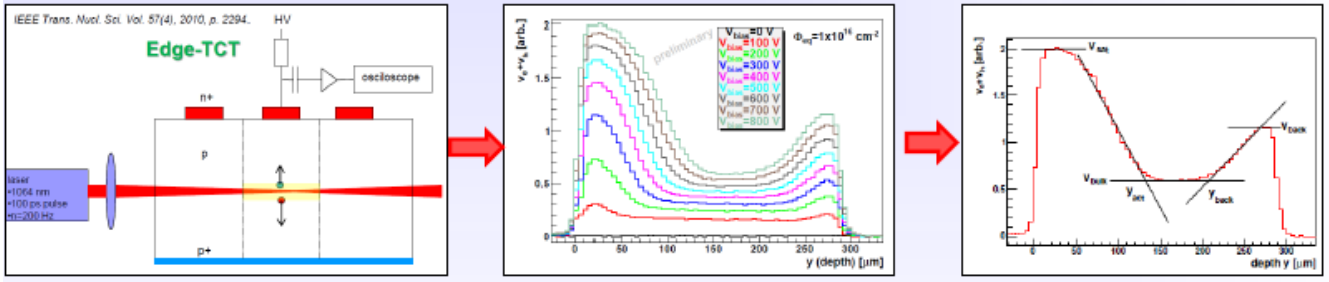
Simulations, with appropriate description of the radiation damage, needed for modelling behaviours at high fluences..

Simulation vs parameterisation

Parameterisation is very accurate to LHC strip fluences. After higher fluences concepts like full depletion do not apply anymore. Trapping and drift voltage penetration are the quantities that better describe the performance of heavily irradiated sensors. RD50 is working to wards making prediction tools for highly irradiated sensors. With both simulation and experimental methods.

- **Parameterization known as e.g. "Hamburg model"**
  - **Leakage current (from IV), Neff (from CV), Trapping times (from TCT)**
  - **Does not include the electric field respectively the double junction effect!**
- **TCAD simulations**
  - **Quite complex and no parameter set that is covering full phase space … reliable?** (silicon materials, different particles, full fluence range, annealing)
- **Parameterization of electric field instead?**
  - Edge-TCT: Extract E-field (more precisely the drift velocity) profile and parameterize it

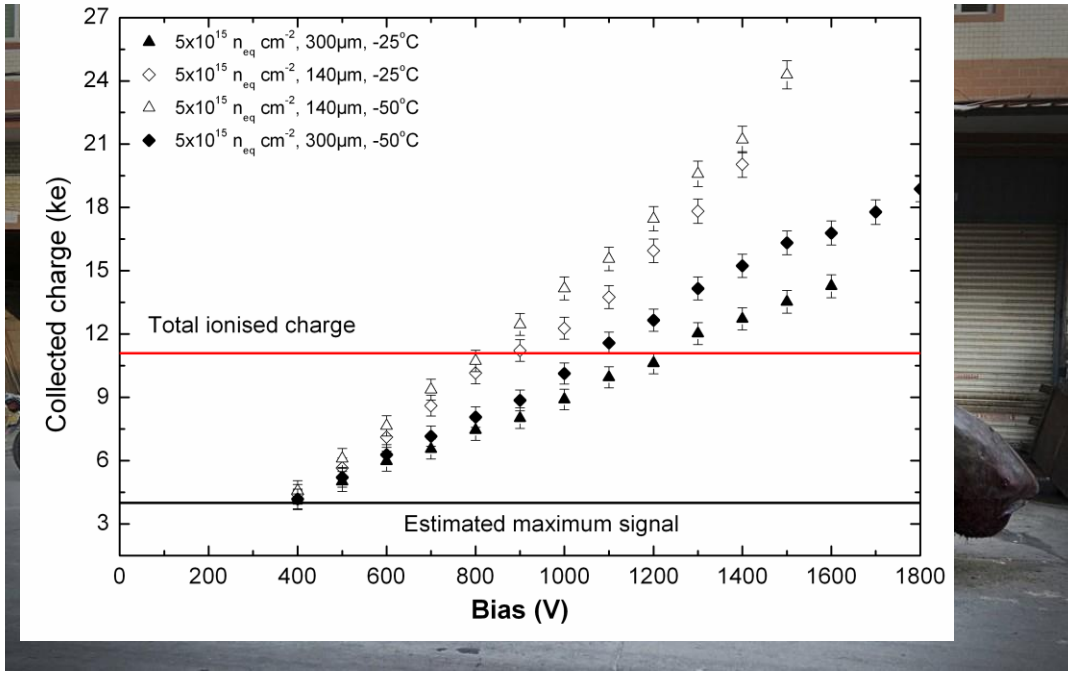
[G.Kramberger et al., PoS (Vertex 2012) 022]



Edge-TCT → Drift velocity profile (v_e+v_h) → fit to extract parameters

RD50 Charge multiplication

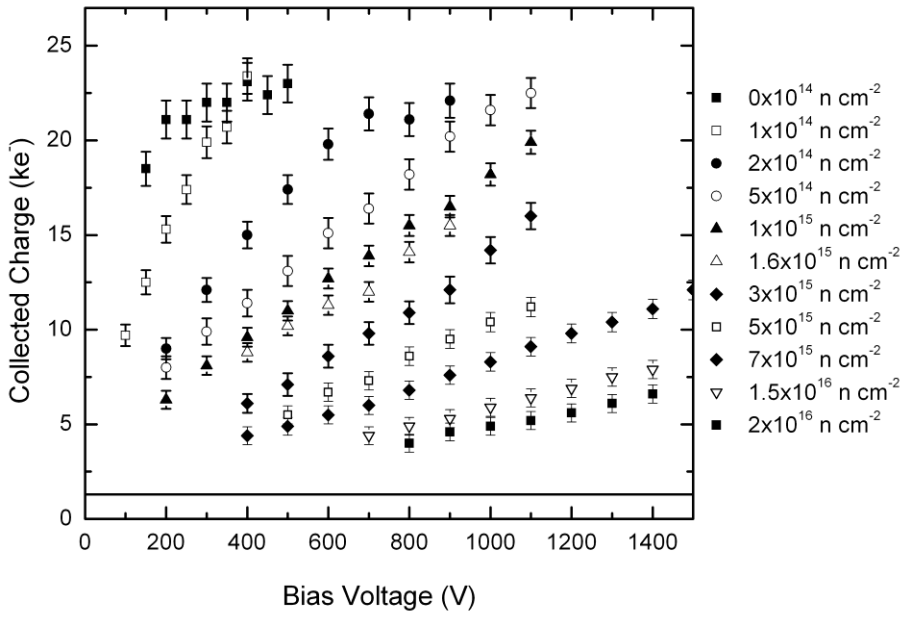
Some times, things go better than planned, a good day out fishing .....



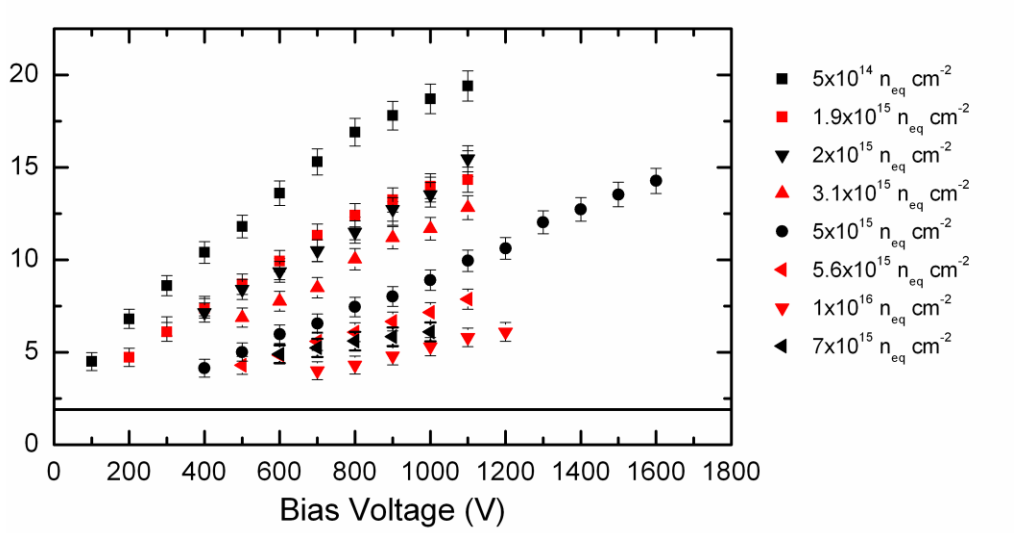
Or more charge than you expect after irradiation .....

Results with proton irradiated 300 μm n-in-p Micron sensors (up to 1x10^{16} n_{eq} cm^{-2})

Irradiated with reactor neutrons



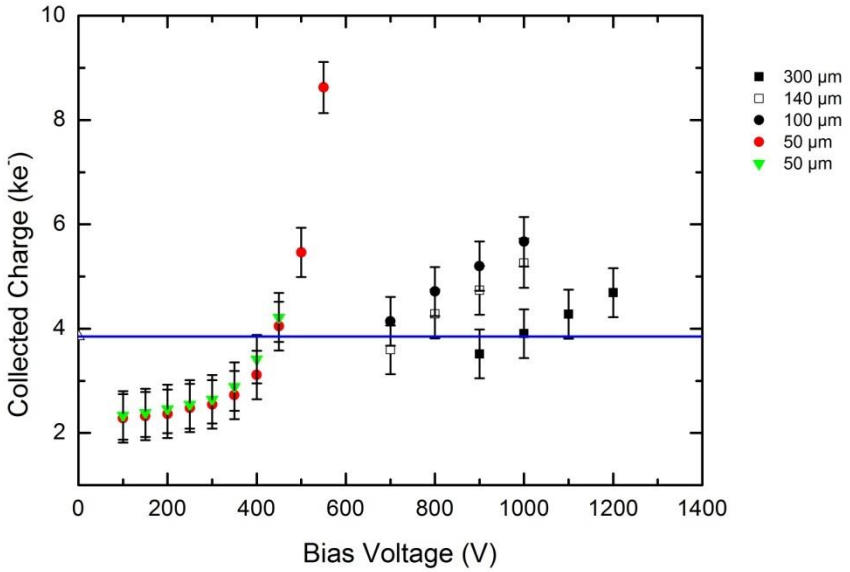
RED: irradiated with 24GeV/c protons
Other: 26MeV protons

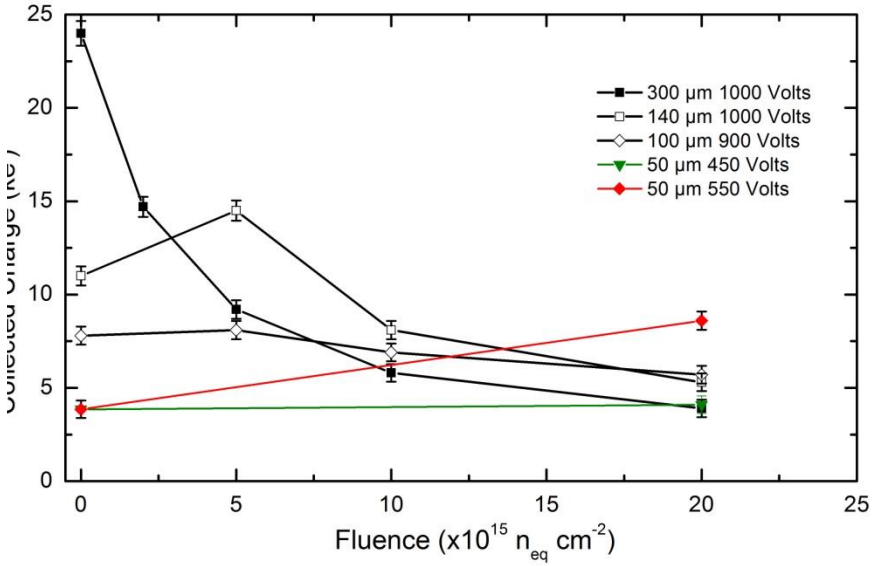


Role of thickness

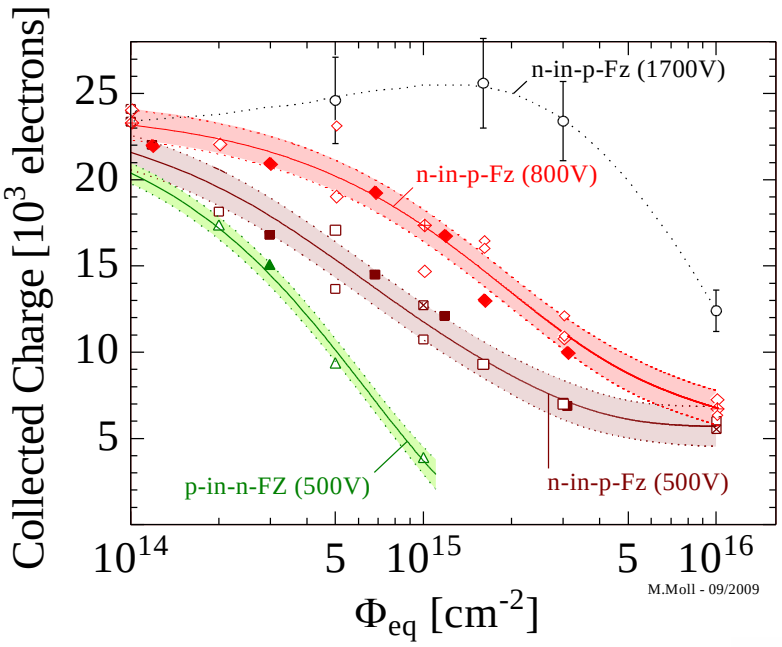
The onset of Charge Multiplication breaks a few rules, like the proportionality of the signal with thickness.....

Charge degradation vs fluence for silicon sensors with different thicknesses





A great margin to gain with extremely high voltage



FZ Silicon Strip Sensors

- n-in-p (FZ), 300µm, 500V, 23GeV p [1]
- n-in-p (FZ), 300µm, 500V, neutrons [1,2]
- n-in-p (FZ), 300µm, 500V, 26MeV p [1]
- n-in-p (FZ), 300µm, 800V, 23GeV p [1]
- n-in-p (FZ), 300µm, 800V, neutrons [1,2]
- n-in-p (FZ), 300µm, 800V, 26MeV p [1]
- n-in-p (FZ), 300µm, 1700V, neutrons [2]
- p-in-n (FZ), 300µm, 500V, 23GeV p [1]
- p-in-n (FZ), 300µm, 500V, neutrons [1]

References:

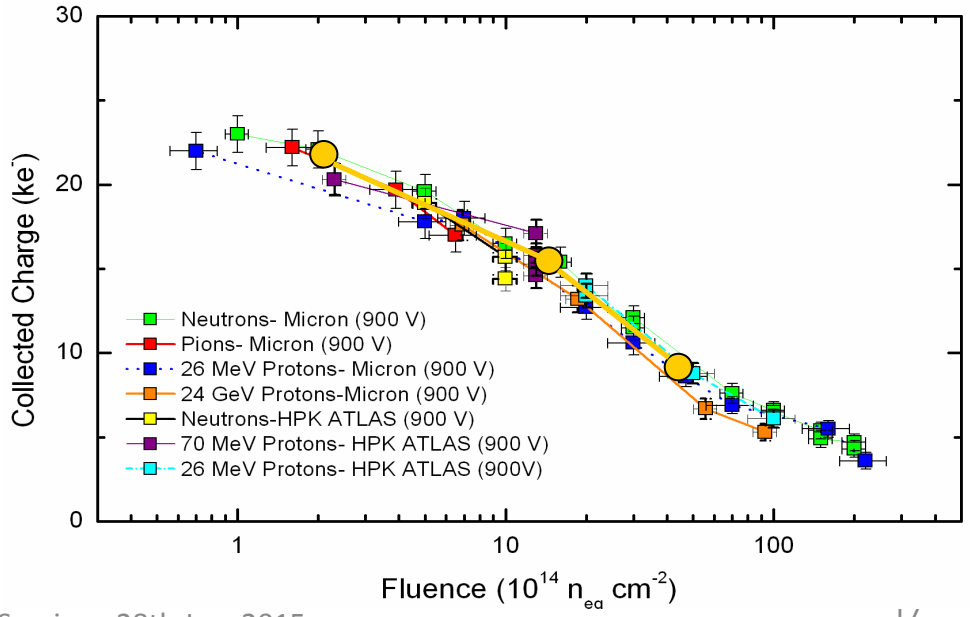
[1] G.Casse, VERTEX 2008
(p/n-FZ, 300µm, (-30°C, 25ns)

[2] I.Mandic et al., NIMA 603 (2009) 263
(p-FZ, 300µm, -20°C to -40°C, 25ns)

Compiled by
M. Moll

..but good agreement among measurements from different groups and sensors from different manufacturers

900 V



Parameterization of Time Resolution

In a simple model approximation, we can write

$$\sigma_t^2 = ([\frac{V_{th}}{S/t_r}]_{RMS})^2 + (\frac{N}{S/t_r})^2 + (\frac{TDC_{bin}}{\sqrt{12}})^2$$

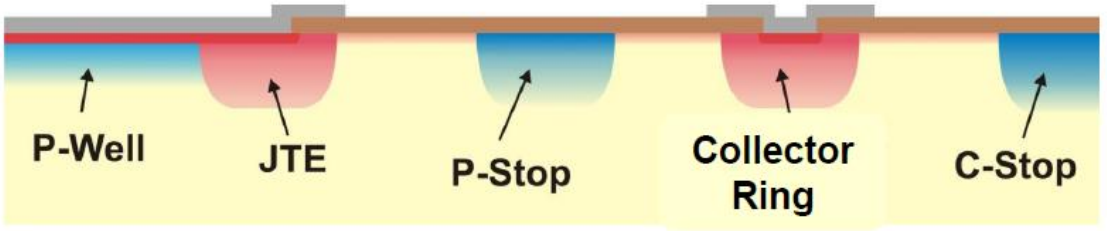
Where:

- S/t_r = dV/dt
- N = system noise
- V_{th} = 10 N

To minimize the time resolution
we need to maximize the S/t_r term
(i.e. the slew rate dV/dt of the signal)

RD50 LGAD New Run. Mask Design

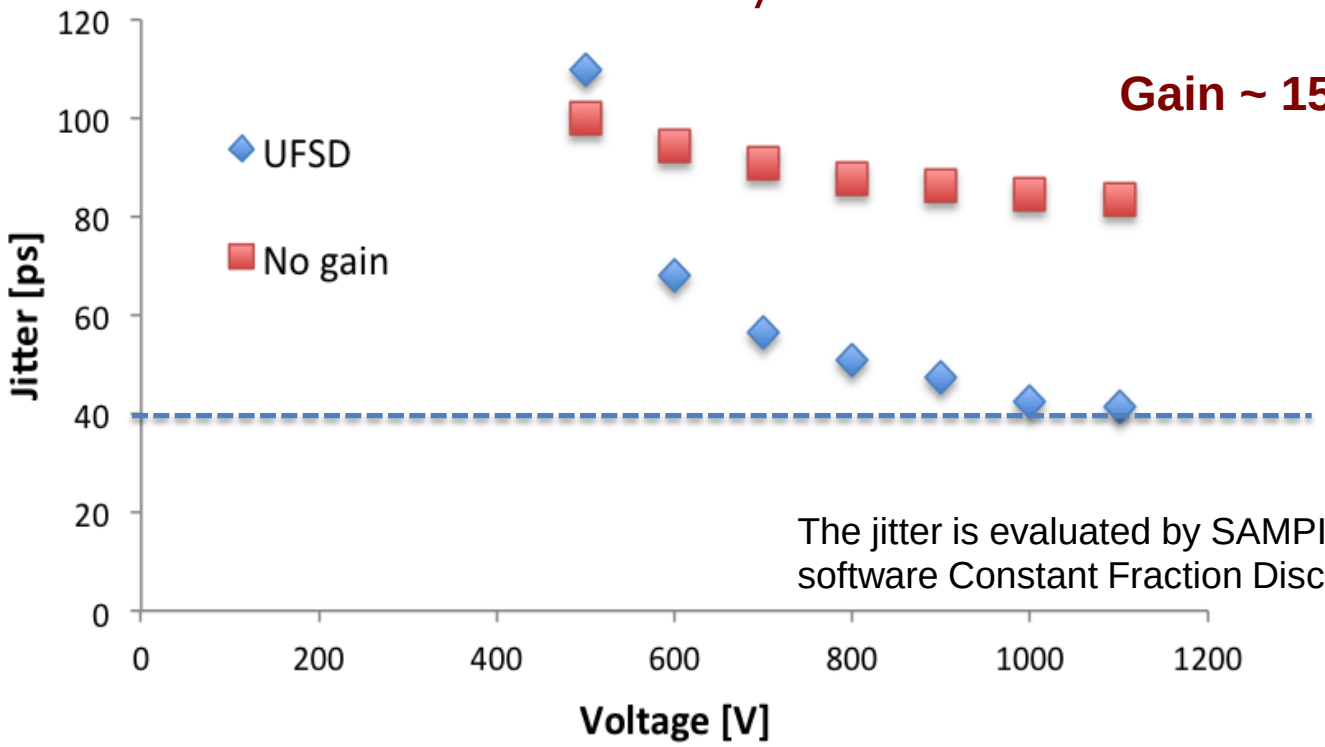
- Pad Detectors with Multiplication
  - ✓ Multiplication Area
    - ❖ **8 x 8** mm
    - ❖ **3 x 3** mm



  - ➢ Termination:* P-Stop + N-Guard Ring
    - * P-Stop + N-Guard Ring with JTE
    - * JTE + P-Stop + N-Guard Ring with JTE
- Pixel Detectors
  - ✓ **1 x 1** mm (6x6 Matrix)
- PIN Diodes (for reference)
  - ✓ **8 x 8** mm
  - ✓ **3 x 3** mm
  - ✓ **1 x 1** mm (6x6 Ma*trix)*
  - ➢ Top & Bottom circular windows in the metal layer.

Time Resolution vs Vbias

Laboratory Results

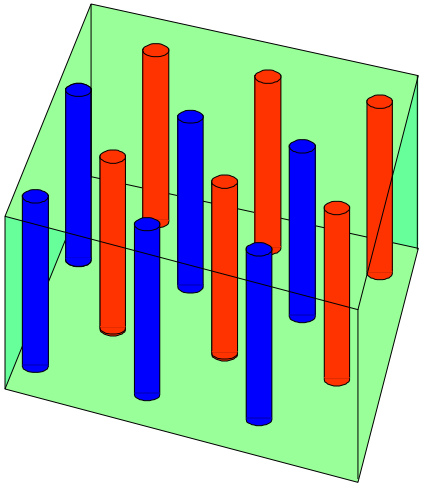


This result is consistent with the simulation predictions:

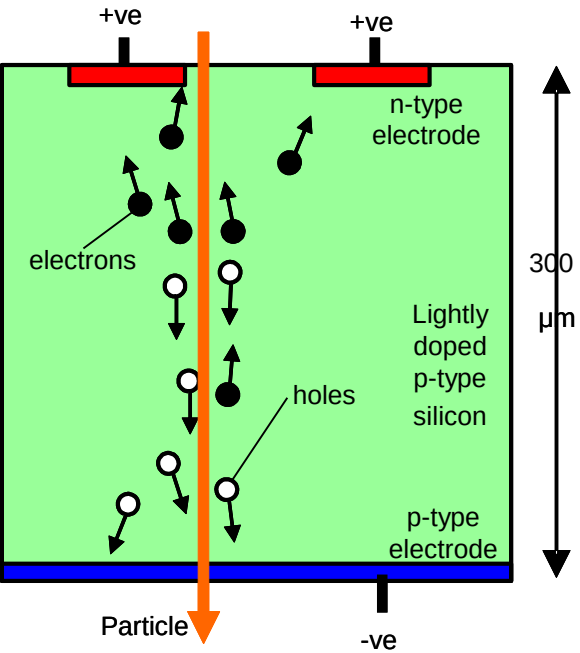
300-micron thick UFSDs with gain of ~ 15 improve by ~ 2 the timing resolution

Different detector structure: 3D Detectors

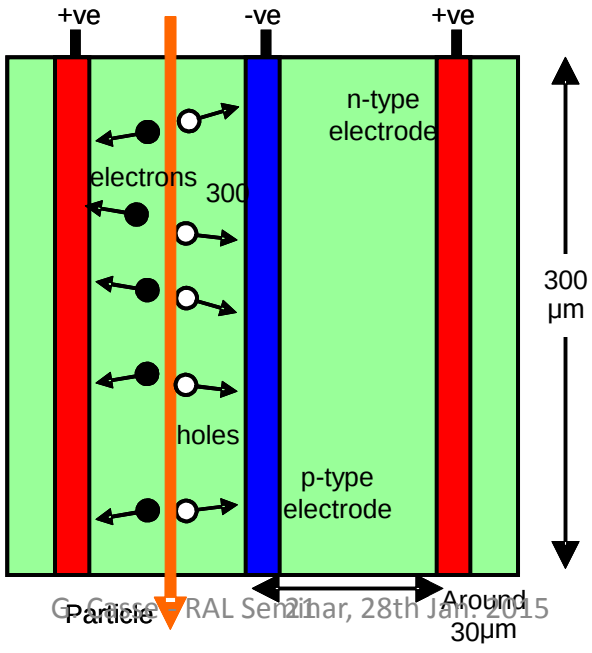
- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30μm:300μm)
- Benefits
  - $V_{depletion} \propto$ (Electrode spacing)^2
  - Collection time $\propto$ Electrode spacing
  - Reduced charge sharing
- More complicated fabrication - micromachining



Planar



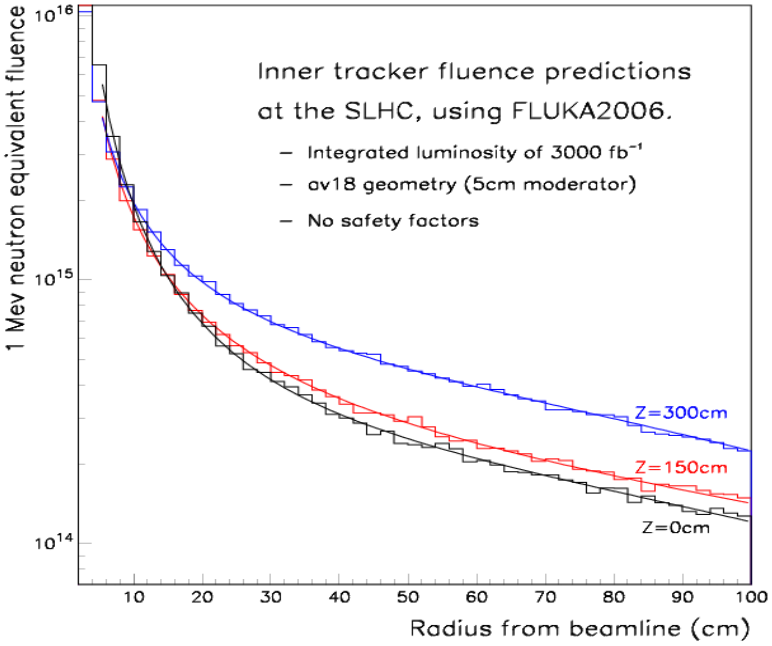
3D



Proposed by S. Parker and C. Kenney of the University of Hawaii in 1995.

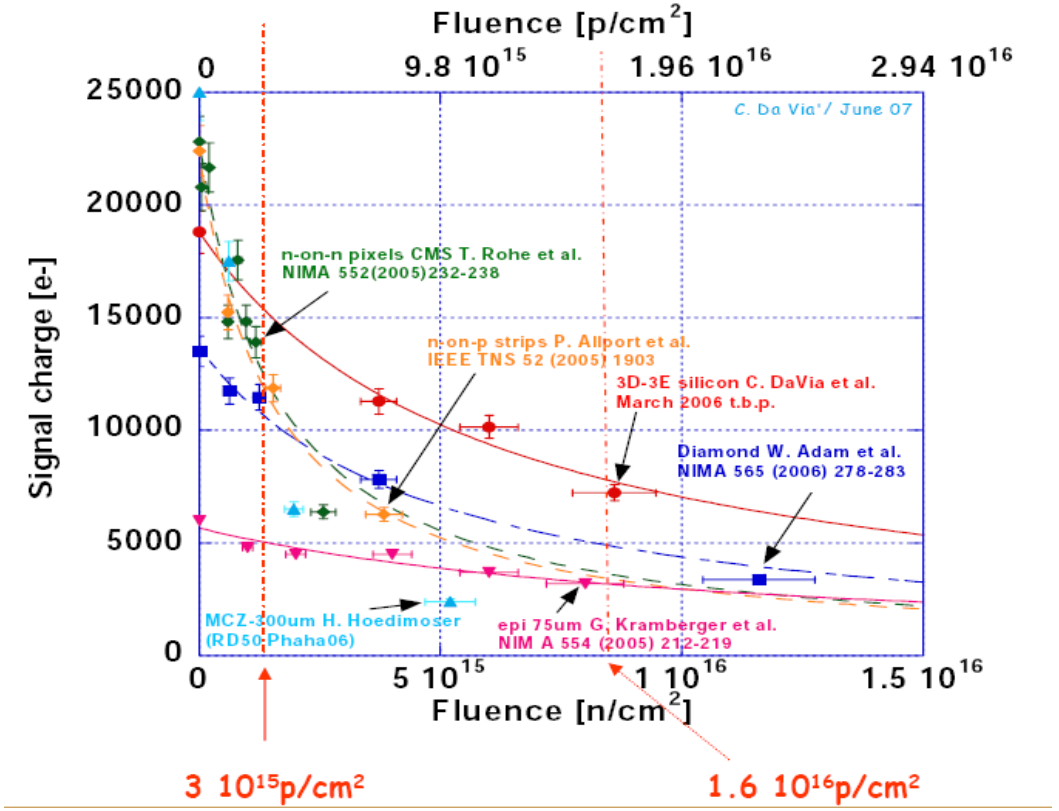
3D sensors radiation hardness

ATLAS



- Super-LHC $L=10^{35}$ $cm^{-2}s^{-1}$
- charged particle dose $10^{16}/cm2$

ATLAS/CMS at 4cm in 3 years
LHCb (lower L) at 8mm in 6 years



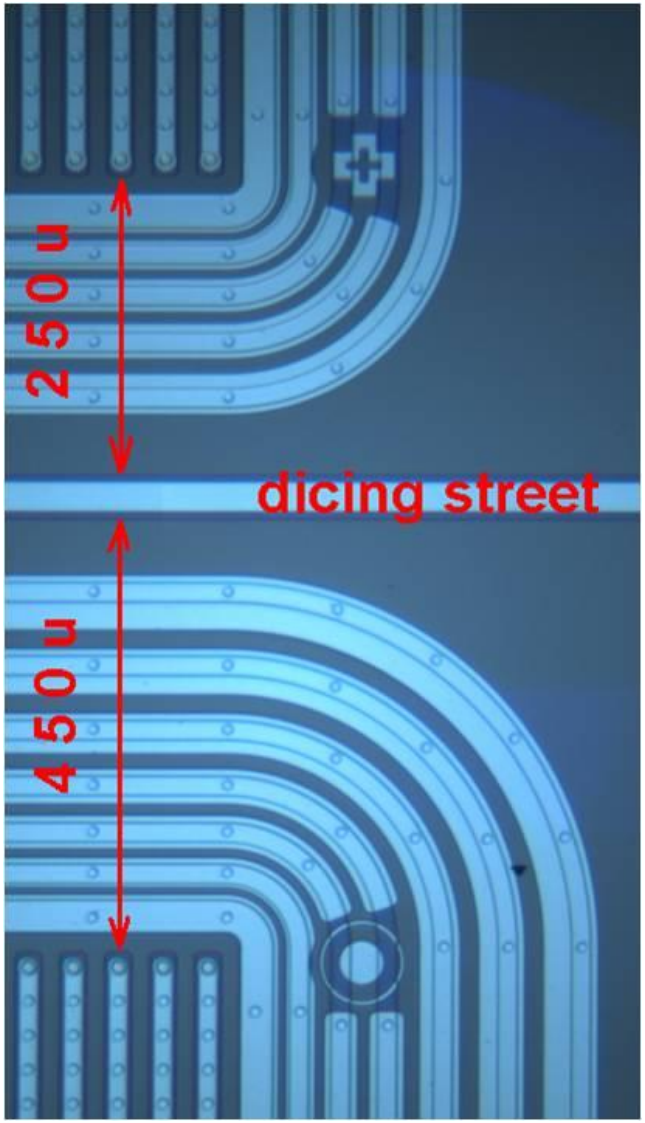
- 3D has highest CCE and at relatively modest Voltages
- …but most difficult fabrication
- **RD50** 3D working group (Richard Bates)
- **ATLAS** 3D working group (Cinzia DaVia)

Current choices for hybridisation

Microstrip detector assemblies

Pixel detector assemblies

Microstrip sensor status

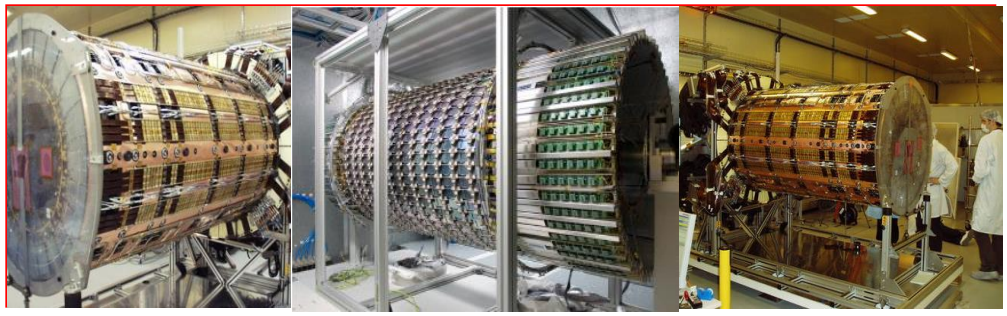


Typical distance between sensitive area and cut edge for high voltage devices ~ 1mm. Lot of interest for reducing this inactive region

Baseline well defined for radiation hardness (according to the results above). Adiabatic improvements been made. Running scenario (temperature, controlled annealing, cooling needs ...) being drafted.

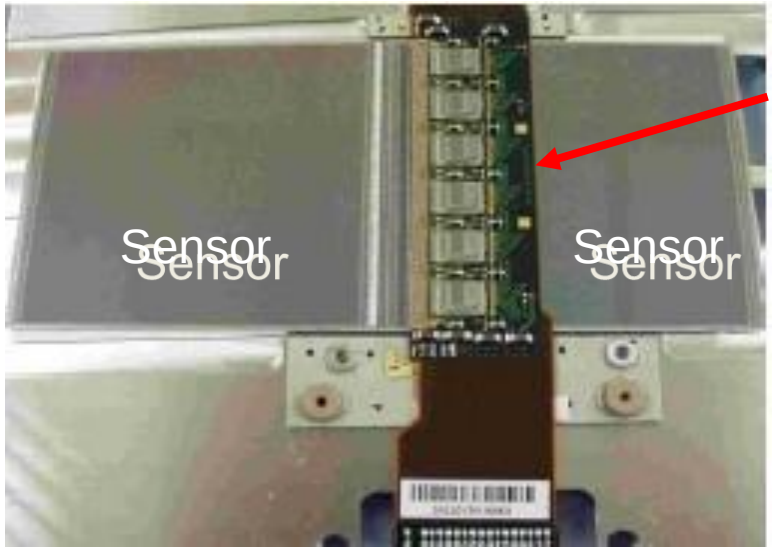
Microstrip sensors

ATLAS Tracker Based on
Barrel and Disc Supports

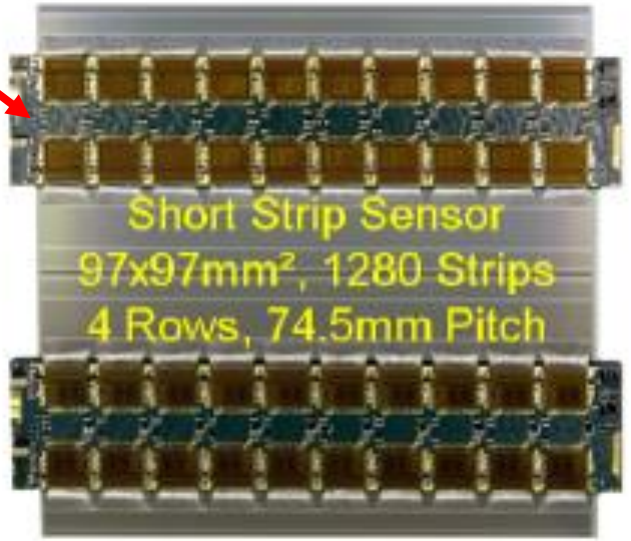


Current barrel-type sensors (768 strips of 80μm pitch per side)

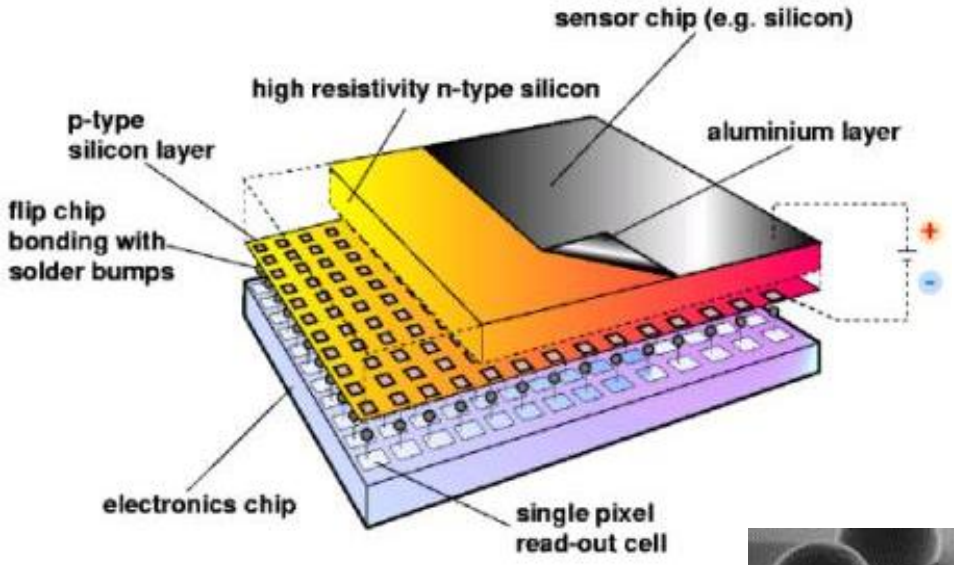
Future barrel-type sensors (1280x4 strips of ~75μm pitch per side)

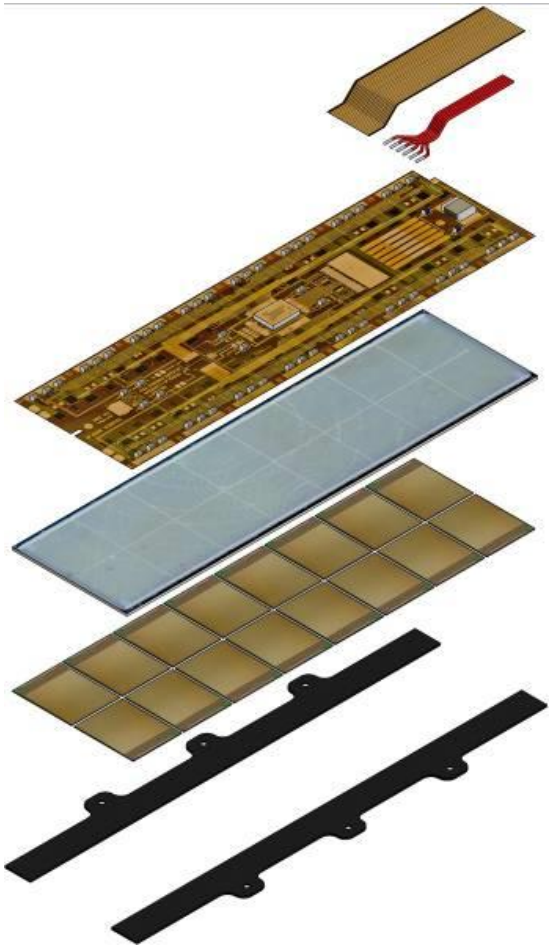


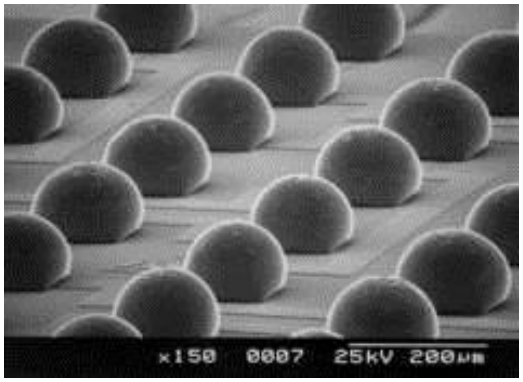
Hybrid cards carrying read- out chips and multilayer interconnect circuit

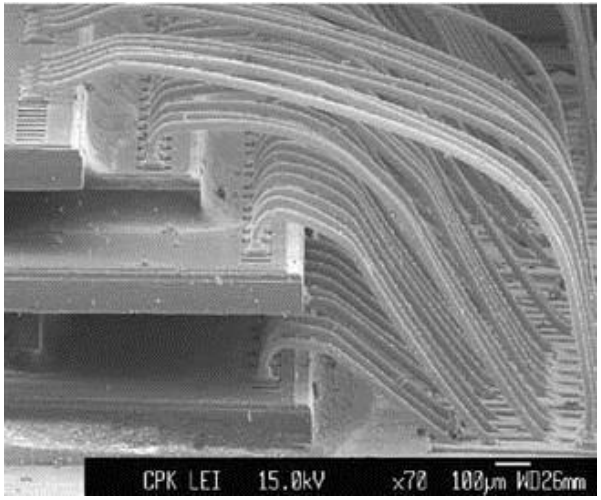


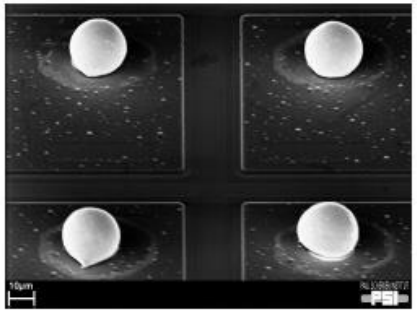
Hybrid pixels





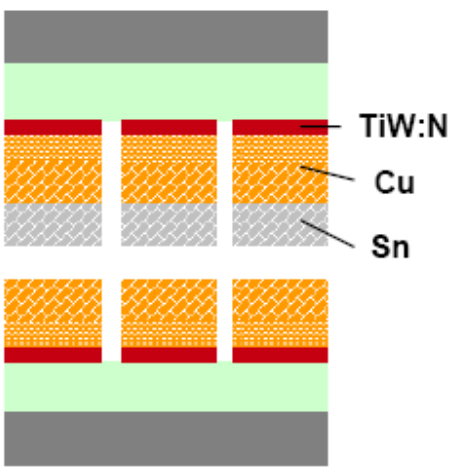




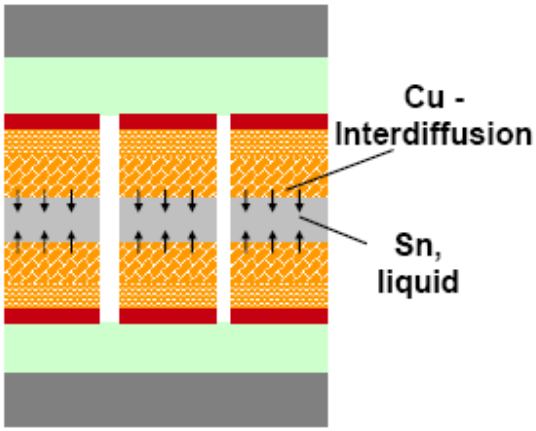


IZM SLID Process

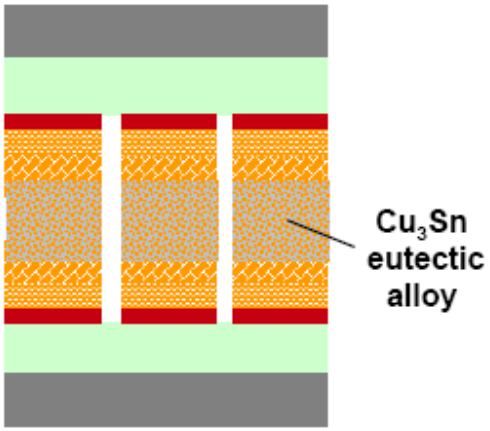
Metallization SLID (Solid Liquid Interdiffusion)



Through Mask Electroplating



Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of Eutectic Alloy;
T_{melt} > 600 °C

- **Alternative to bump bonding (less process steps "low cost" (IZM)).**
- **Small pitch possible (<< 20 μm, depending on pick & place precision).**
- **Stacking possible (next bonding process does not affect previous bond).**
- **Wafer to wafer and chip to wafer possible.**

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

Detector requirements for different collider types

Super-B factories, Linear colliders, ALICE.
These all will have similar **requirements**:

- Low mass (detector and services)
- High granularity
- Speed
- Radiation hard (to doses much lower than hadron colliders)

Example:

Parameter	LHC	ILC	ILC/LHC performance
Sensitive time window	25 ns	~50 ms	$\sim 10^{-3}$
Radiation resistance	~20 Mrads	~100 krad	$\sim 10^{-2}$
Tracking precision	~45 μm	~3 μm	15
Layer thickness	2 % X_0	0.1% X_0	20

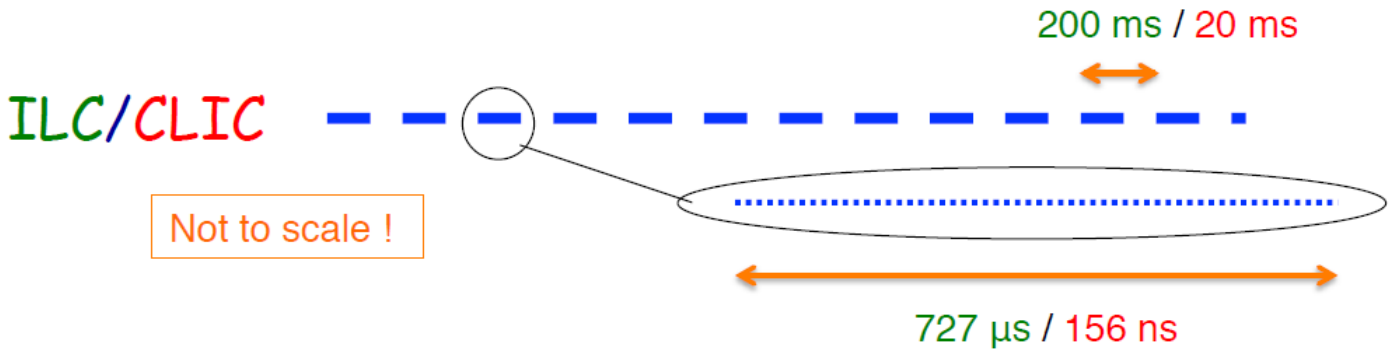
ILC and CLIC machine environment

	ILC at 500 GeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	$2x10^{34}$	$6x10^{34}$
BX separation	554 ns	0.5 ns
#BX / train	1312	312
Train duration	727 µs	156 ns
Train repetition rate	5 Hz	50 Hz
Duty cycle	0.36%	0.00078%
σ_x / σ_y (nm)	474 / 6	≈ 45 / 1
σ_z (µm)	300	44

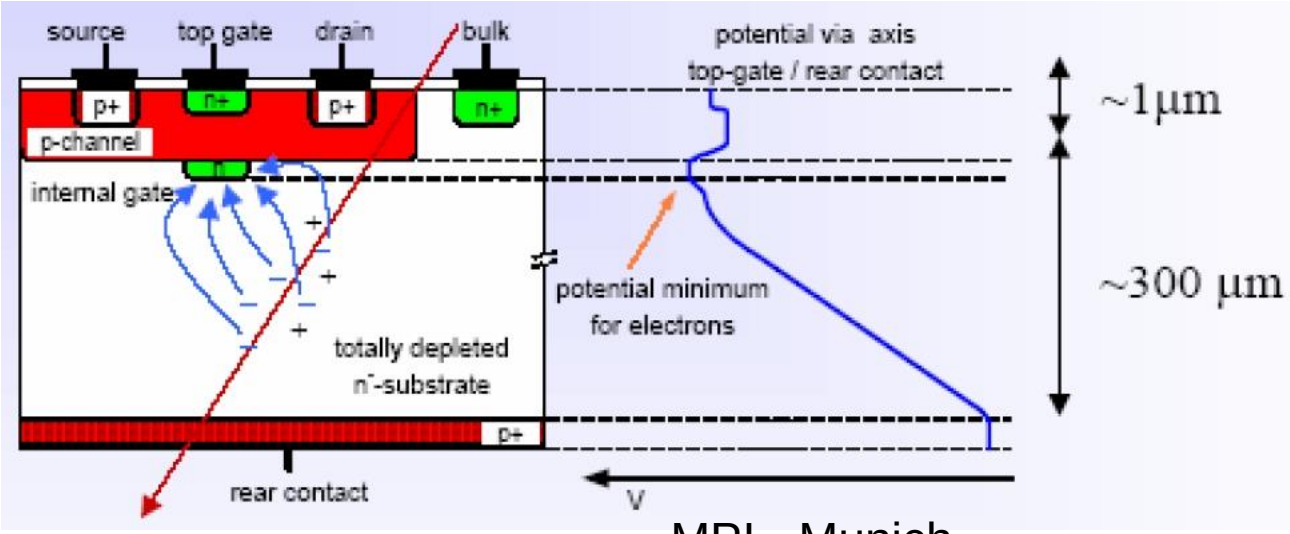
ILC ESD-2012/2 / CLIC CDR

drives timing requirements for detectors

very small beam sizes → high rates of e^+e^- and hadronic backgrounds

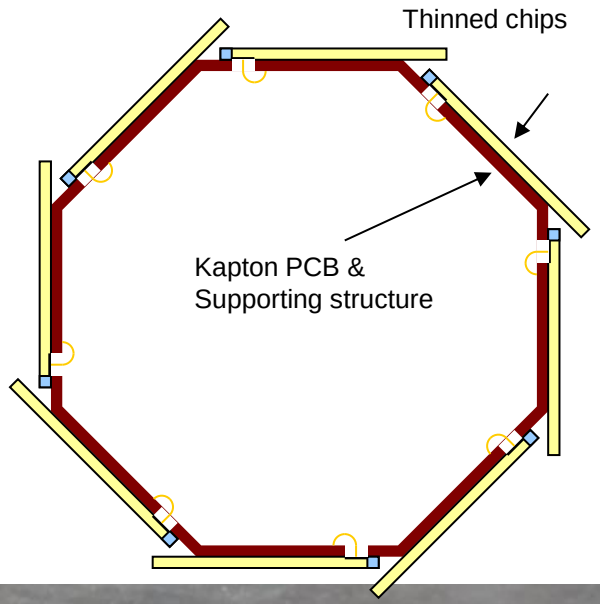


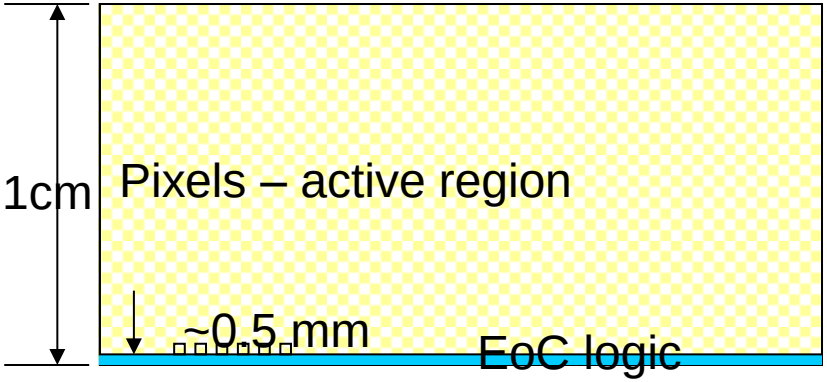
Detector concepts: DEPFET Pixel Detectors

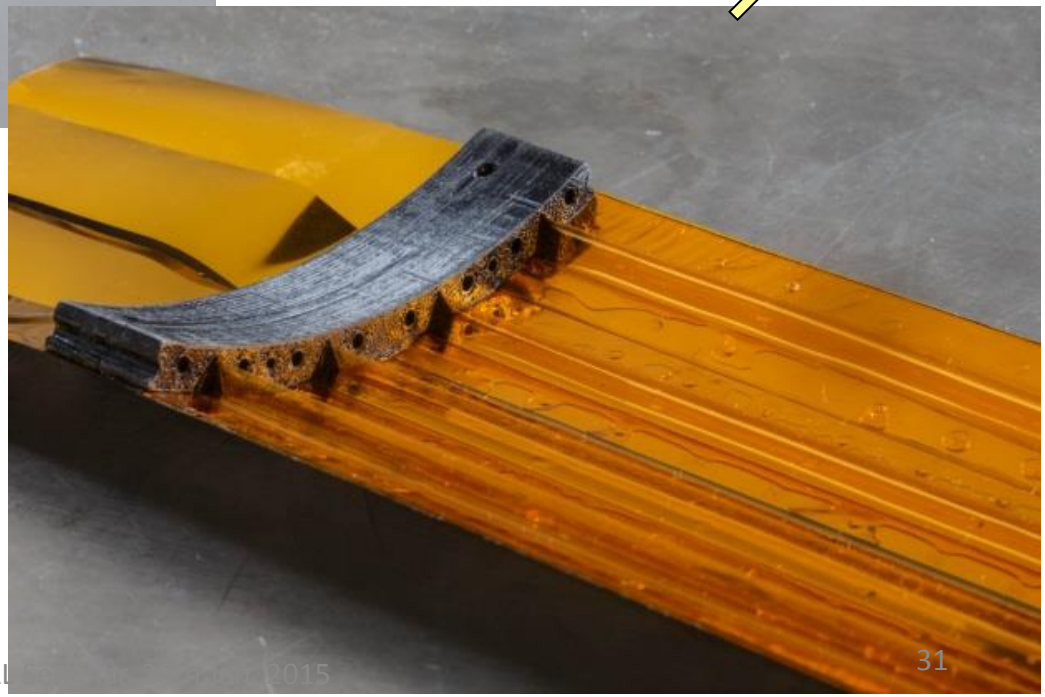


MPI - Munich

The DEPFET detector is a detector with internal amplification. The n-bulk is fully depleted with a potential minimum below the strips and the structure of a field effect transistor. The electrons created by a charged particle accumulate in the potential minimum. The field configuration is such that the electrons drift underneath the gate of the transistor modifying the source drain current. An active clear is necessary to remove the electrons.

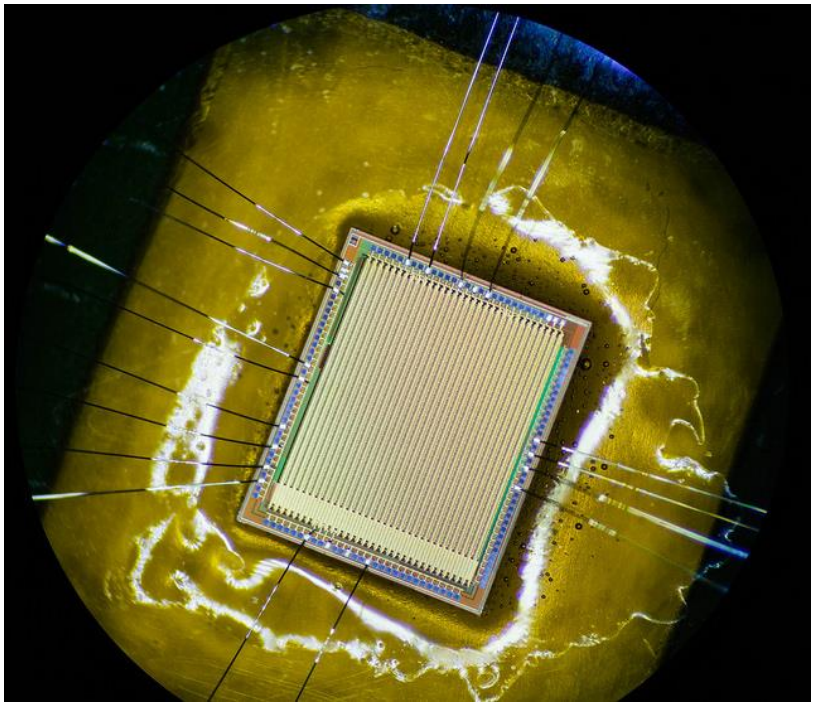

Thinned chips
Kapton PCB &
Supporting structure

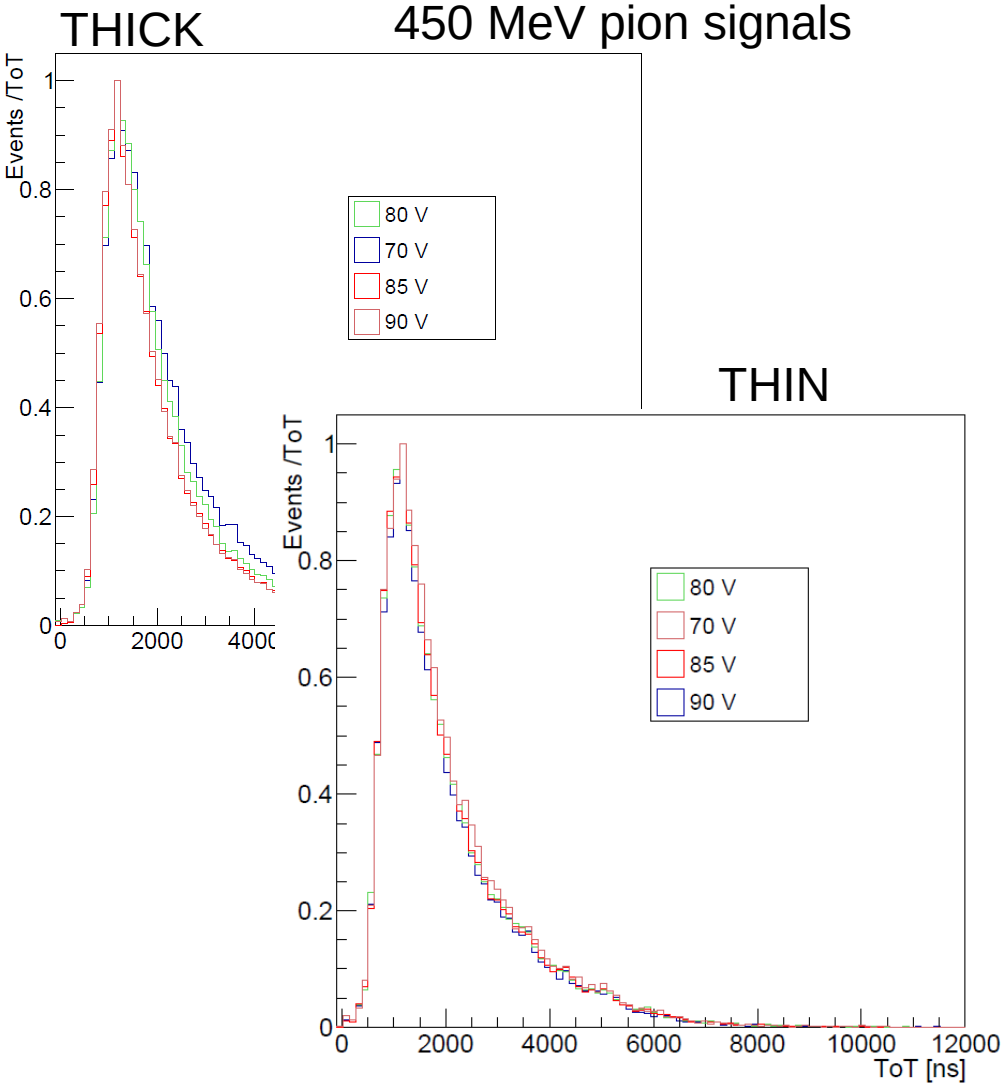

1cm
Pixels – active region
~0.5 mm
EoC logic



Thin detectors

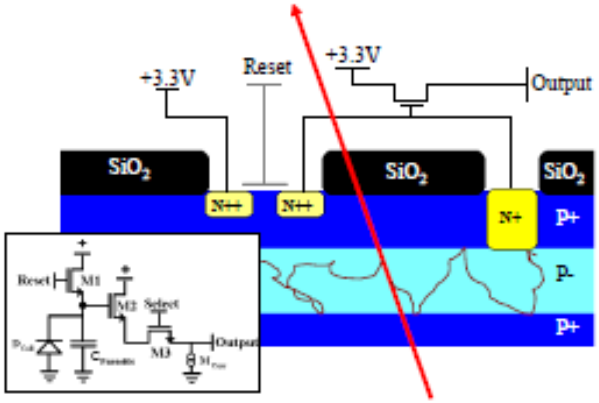
- Chips have been thinned to < 100 µm and successfully tested

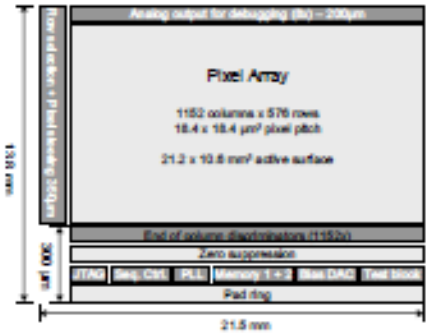


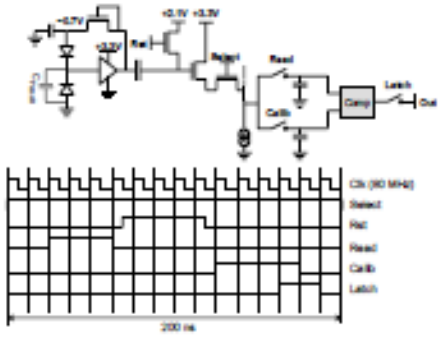


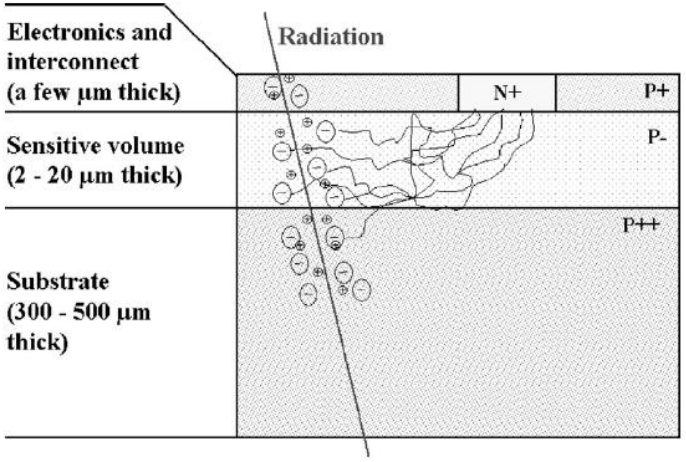
Monolithic Active Pixels

MAPs, **standard CMOS processing**. Active pixel cell with an NMOS transistor. The N-well collects electrons from both ionization and photo-effect.



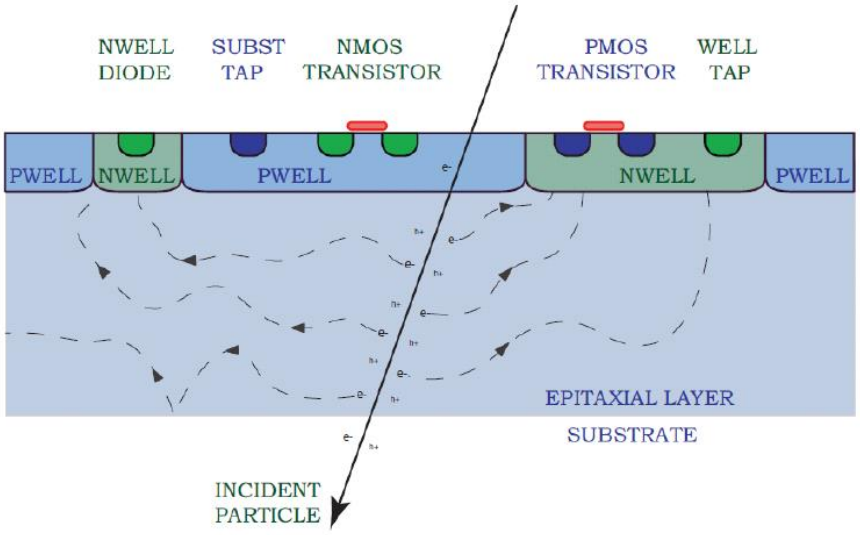


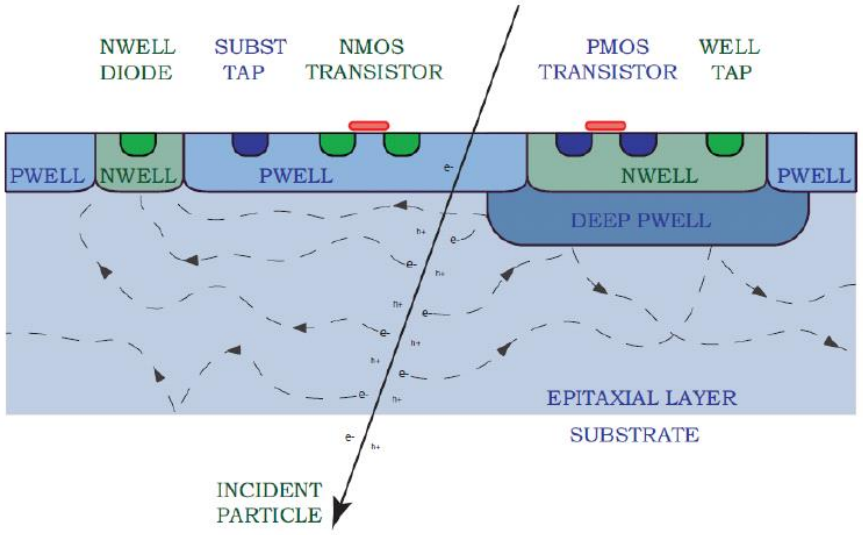




QUADRUPLE WELL MAPS

- QUADRUPLE WELL MAPS pixel = isolation of electronics (water) from detector (oil),
  (potentially thicker active layer and operation in depletion),
- Attempt of:
  - increasing collection efficiency and collection speed ➡ radiation hardness
  - making detector ”active” – processing of signals in situ ➡ being able to cope with required timings
- Large area with stitching, but fetaures: radiation hardness, collection efficiency are not perfect





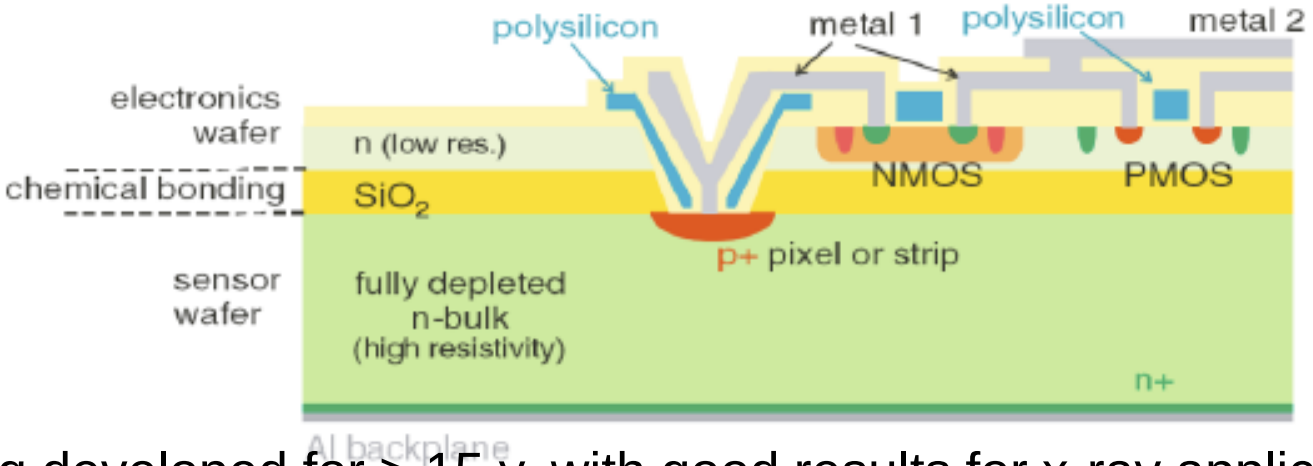
- Good for 3T pixel design, no processing in pixel,
  uncomplicated pixel = good for yield of large devices,

Renato Turchetta 2010 IEEE NSS&MIC (RAL),
Ping Yang Pixel2014 (CCNU, CERN)

Monolithic Active Pixels

SOI: silicon on insulator

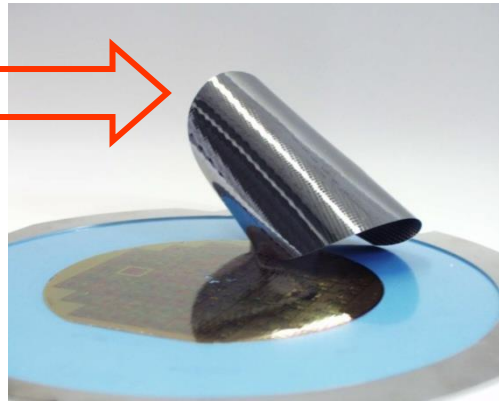
A SOI detector consists of a thick full depleted high resitivity bulk and separated by a layer of SiO2 a low resistivity n-type material. NMOS and PMOs transistors are implemented in the low resitivity material using standard IC methods.



SOI is being developed for > 15 y, with good results for x-ray applications. Does not exhibit yet sufficient radiation tolerance for tracking.

One of the main feature of MAPS

Can be very thin (~25 µm of silicon in total) and still fully efficient!

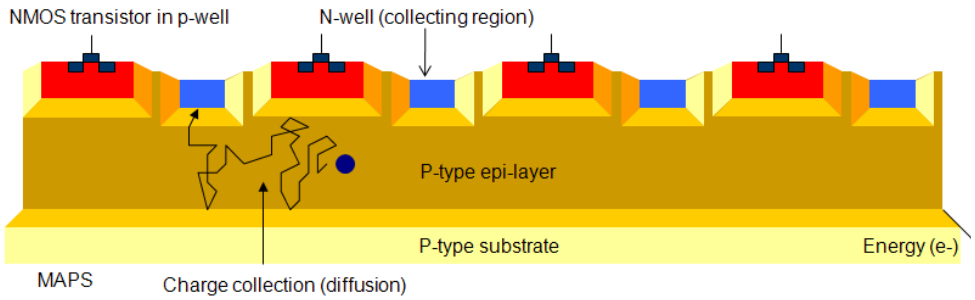


Problem: how to handle, interconnect and at the end built a low mass ladder with such a thin device?

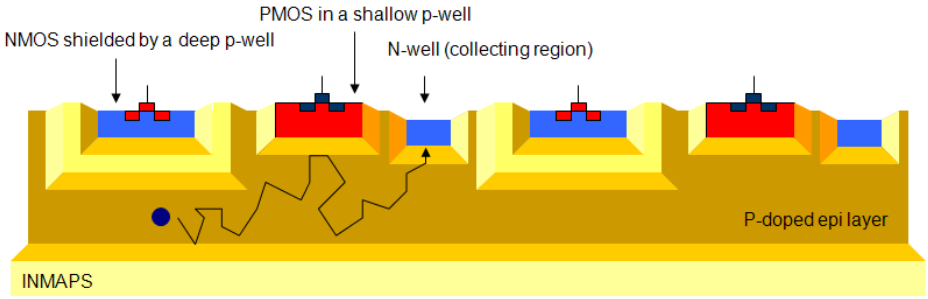
Speeding up the CMOS: HV-CMOS

- CMOS pixel flavors (five years ago)

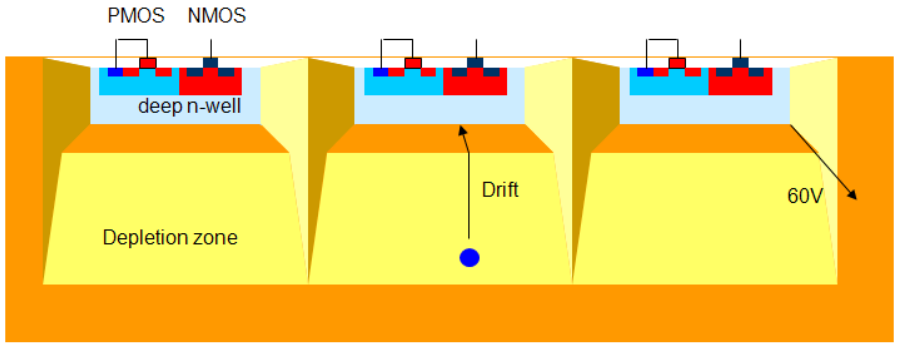
Standard MAPS



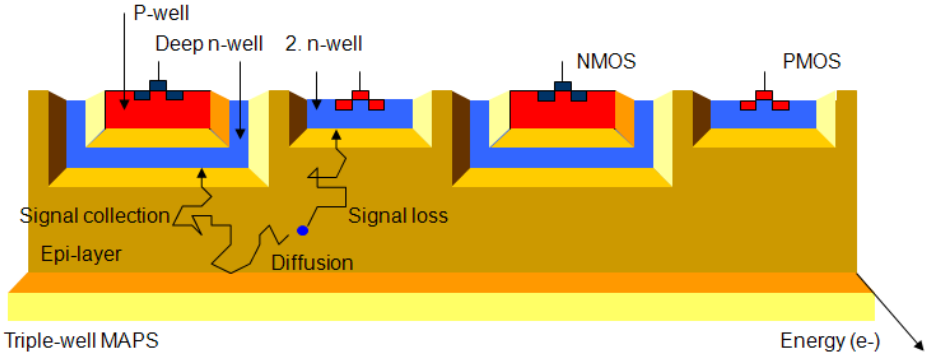
INMAPS



HVCMOS



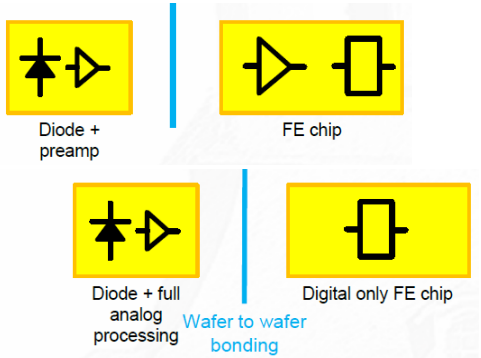
TWELL MAPS

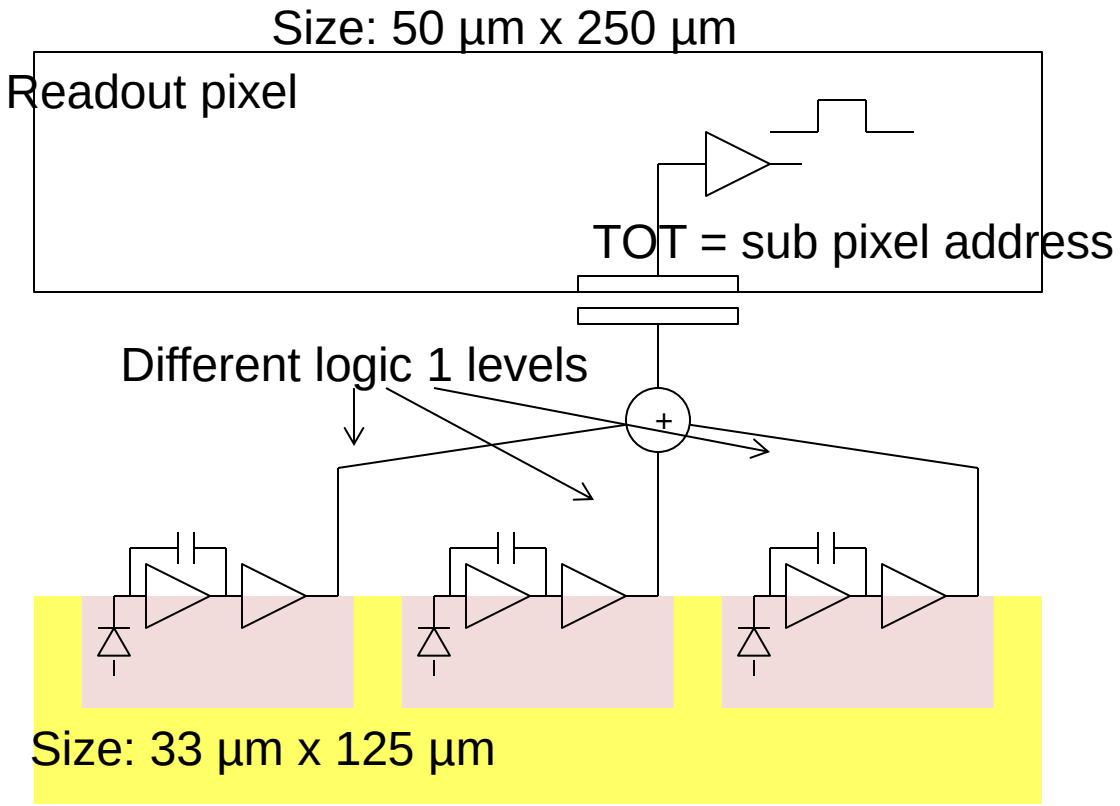


Possible HVCMOS for ATLAS Pixels

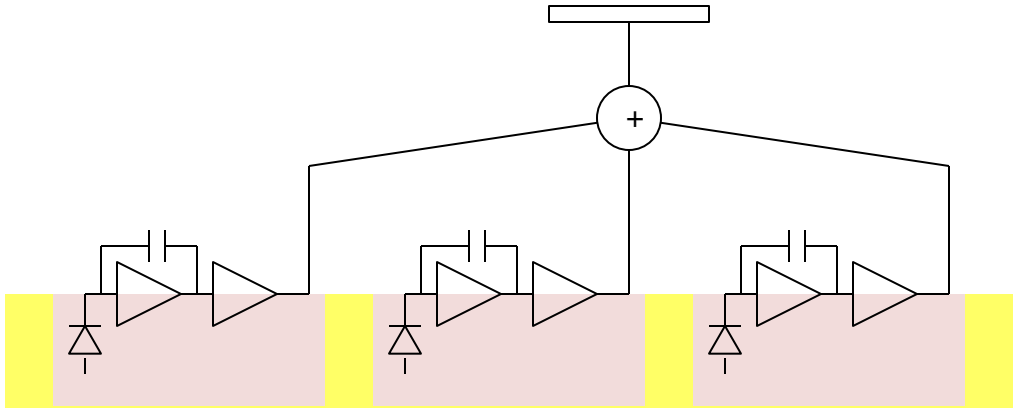
- To be coupled to readout digital elec
- Digital outputs of three pixels are multiplexed to one pixel readout cell
- HVCMOS pixel contains an amplifier an comparator

- Hybrid Pixels with "smart" diodes:
  - HR- or **HV-CMOS** as a sensor (8")
  - Standard FE chip
  - CCPD (HVCMOS) on FE-I4
- CMOS Active Sensor + Digital R/O chip
  - HR- or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated **"digital only" FE chip**

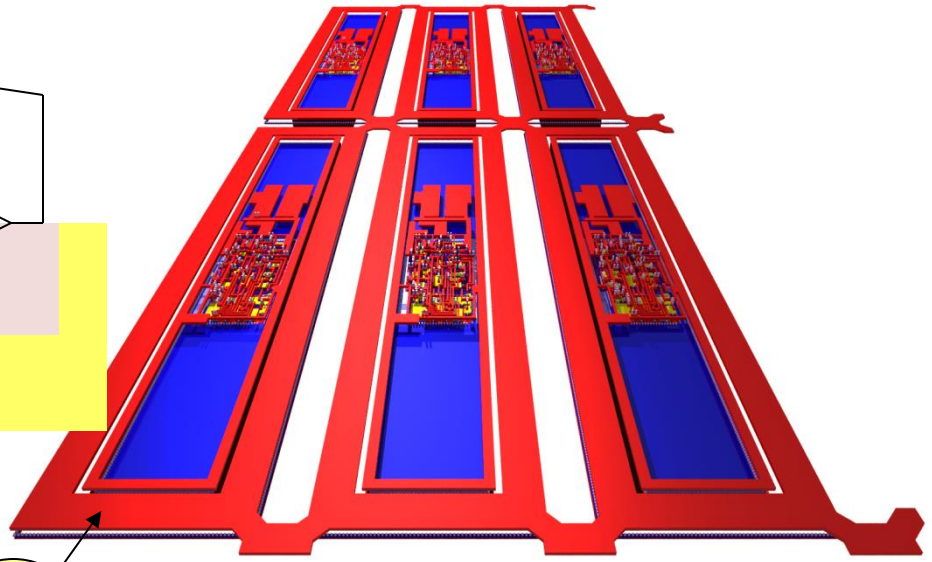




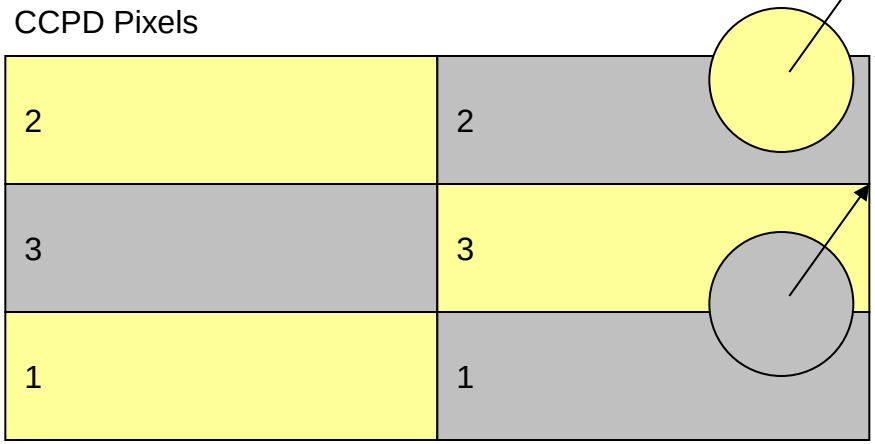
CCPD detector (HV2FEI4) I. Peric, CPIX – Bonn, Sep. 2014

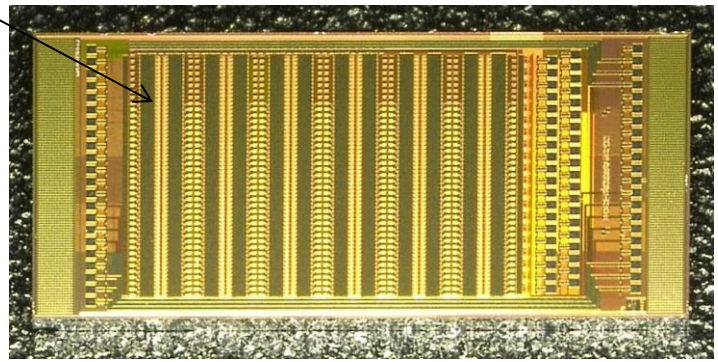


Size: 33 µm x 125 µm



CCPD Pixels

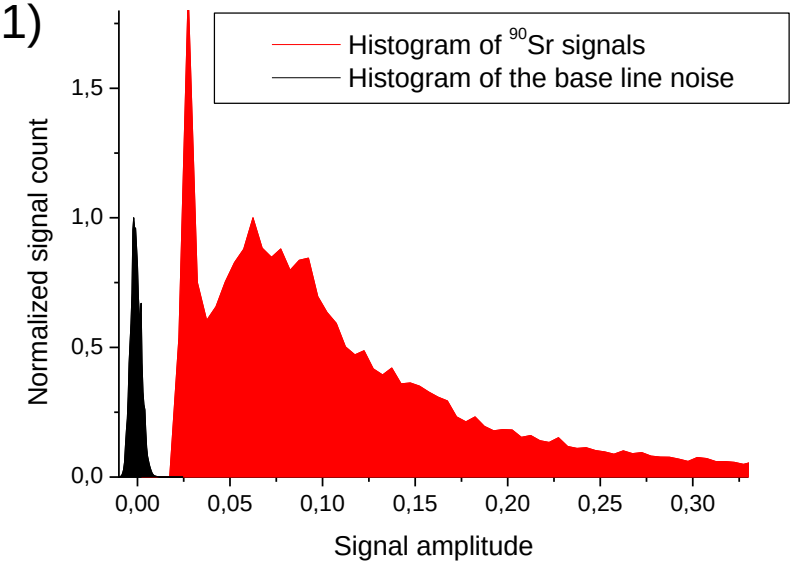


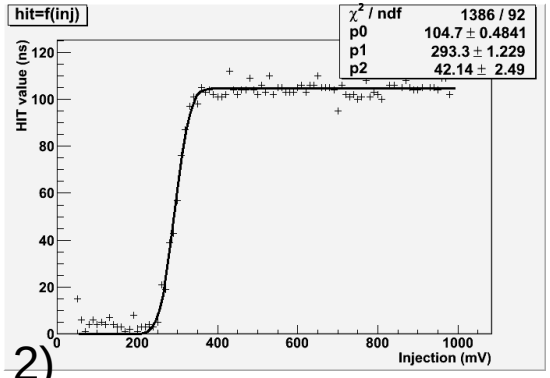


Results

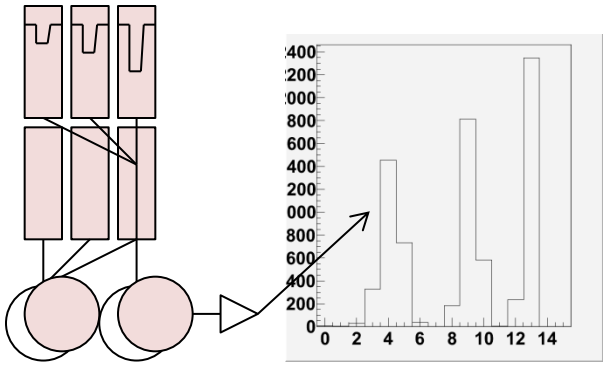
1) CCPDv1: SNR after neutron irradiation at Jozef Stefan Institute 10^{15} n_{eq}/cm^2 ~20 (5C, -55V bias) (Signal ~ 1180e) (measured 2014) (Unirradiated chip @ -50V bias: 1600e)
2) CCPDv2: works after 862 Mrad (x-ray irradiation CERN) (noise at room temperature 150e)
3) CCPDv1: sub pixel encoding works measured for one pixel – still needs optimization

1)





2)

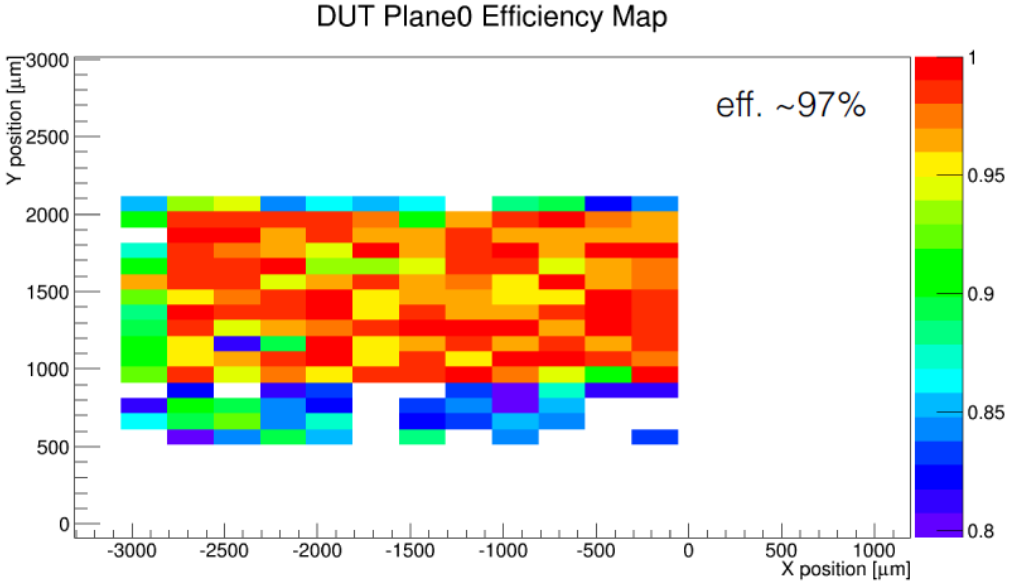


3)

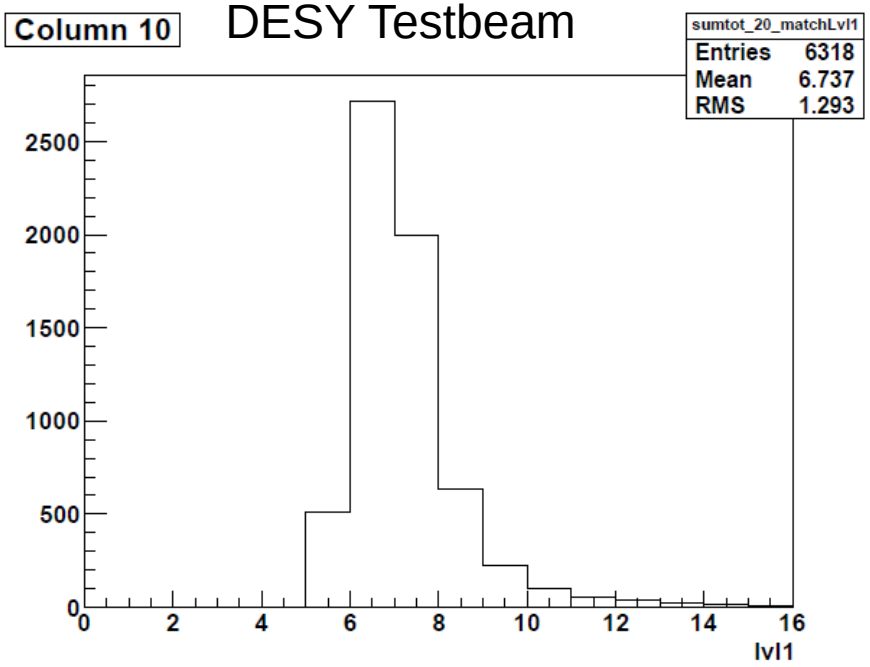
Results

CCPDv2 and v1: test beam measurements in 2013(DESY) and 2014 (PS): efficiency 97%
Sub pixel coding not used
Timing still not as needed

PS Testbeam



DESY Testbeam



Micro-strips in HV-CMOS

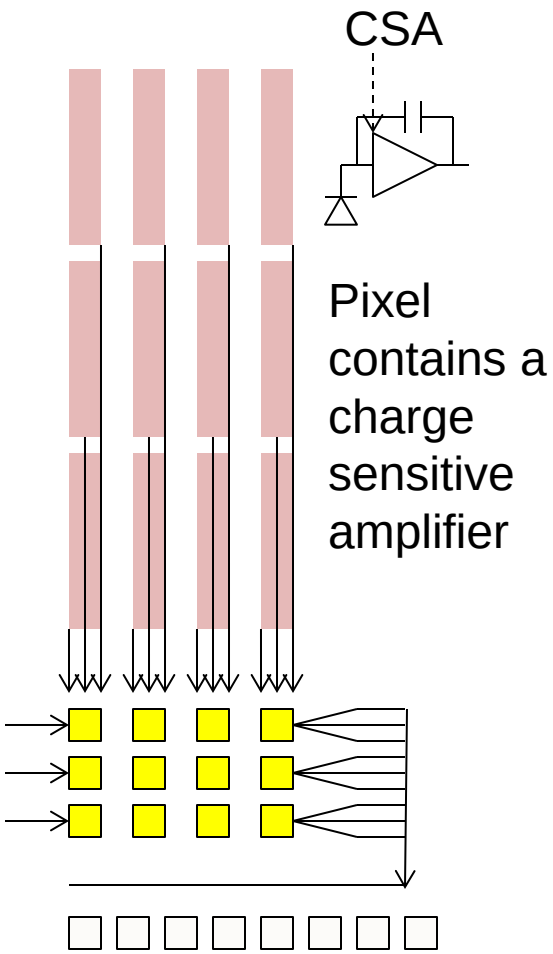
HVCMOS for ATLAS strip layers

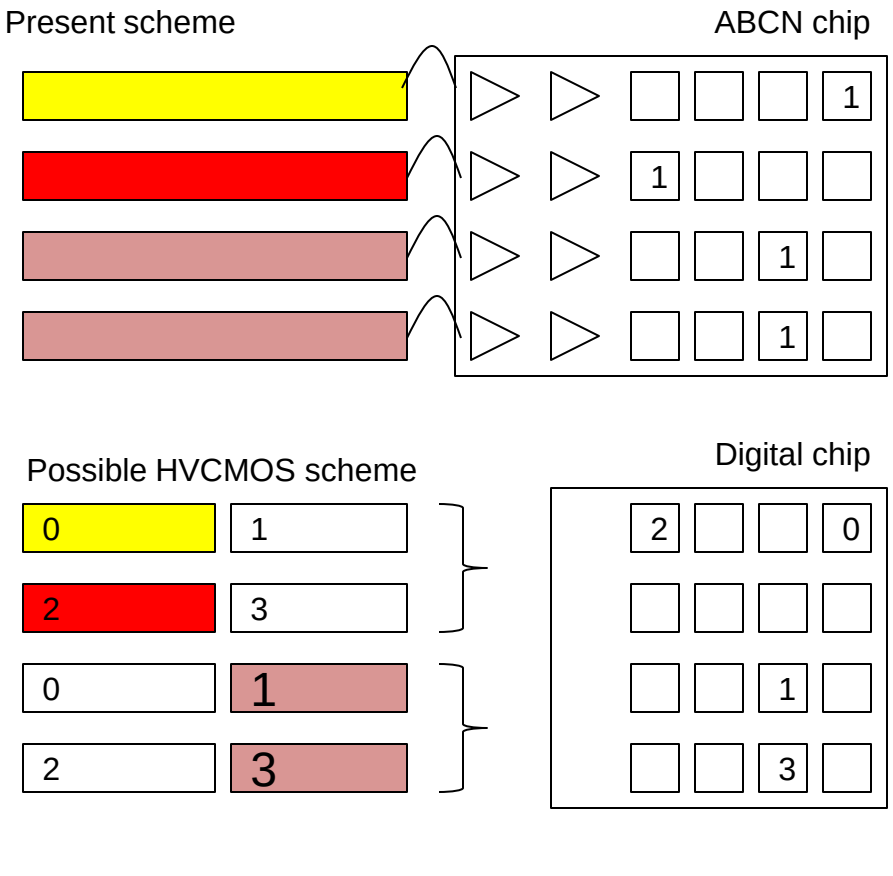
One of possible concepts: Strips are segmented into (long) pixels. Every pixel has its own readout cell, placed on the chip periphery

The periphery generates pixel addresses with a constant delay respecting the hit

Redundant address lines used to cope with simultaneous hits

Strip readout chip (like ABCN) replaced by a purely digital chip (based on existing digital parts)

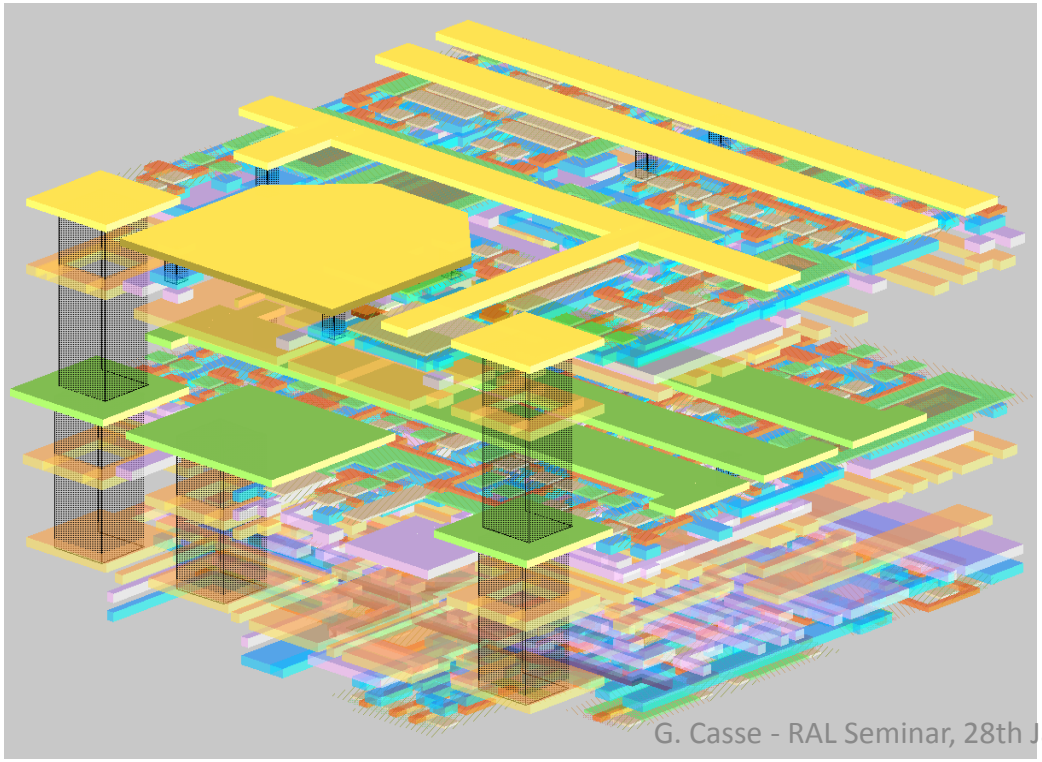




Ultimate Interconnection: Vertical Integration

Ideal solution for reducing material and easing assembly in detector system is to integrate electronics and sensors into a single item … if affordable

- This has been a “dream” for many years
- More complex detectors, low mass
- Liberate us from bump/wire bonding



Many different aspects of these new technologies such as SLID (solid liquid inter-diffusion), TSV (through silicon vias), ICV (inter-chip vias) as well as more highly integrated concepts.

Commercial technologies becoming available for custom design:
IBM, NEC, Elpida, OKI, Tohoku, DALSA, Tezzaron, Ziptronix, Chartered, TSMC, RPI, IMEC……..

But are they all, or even, are any technologies radiation hard?

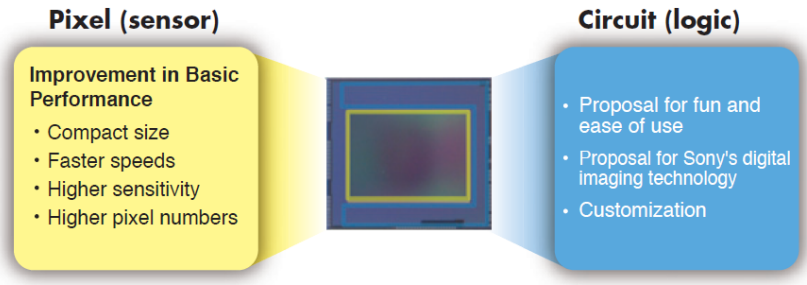
How does see it industry?

Sony's Stacked CMOS Image Sensor Solves All Existing Problems in One Stroke

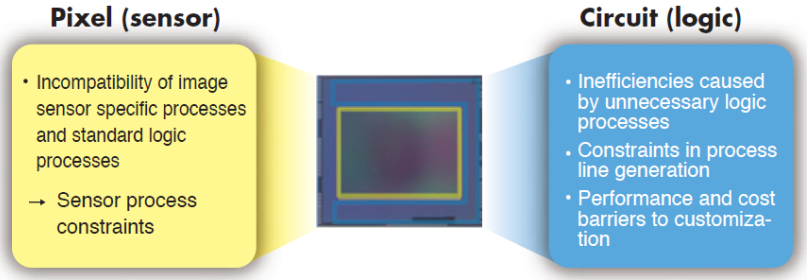
In conventional CMOS image sensors, the pixels (sensors) and circuits (logic) are formed on the same silicon substrate.
Like oil and water, this coexistence of two conflicting elements makes it difficult to optimize their characteristics and also imposes other constraints.
The "stacked CMOS image sensor*1", a new generation of the back-illuminated CMOS image sensor, developed by Sony solves these problems in one stroke.
Stacking the pixel section and the circuit section enables compact size, high image quality, faster speeds and flexible integration of versatile functions.
Through this technology, Sony has created functions that will enable differentiation of final products to provide new ways of enjoying images.

*1: See press release at: http://www.sony.net/SonyInfo/News/Press/201201/12-009E/

■ Figure 1 Demands by Customers that Use Image Sensors in Final Products



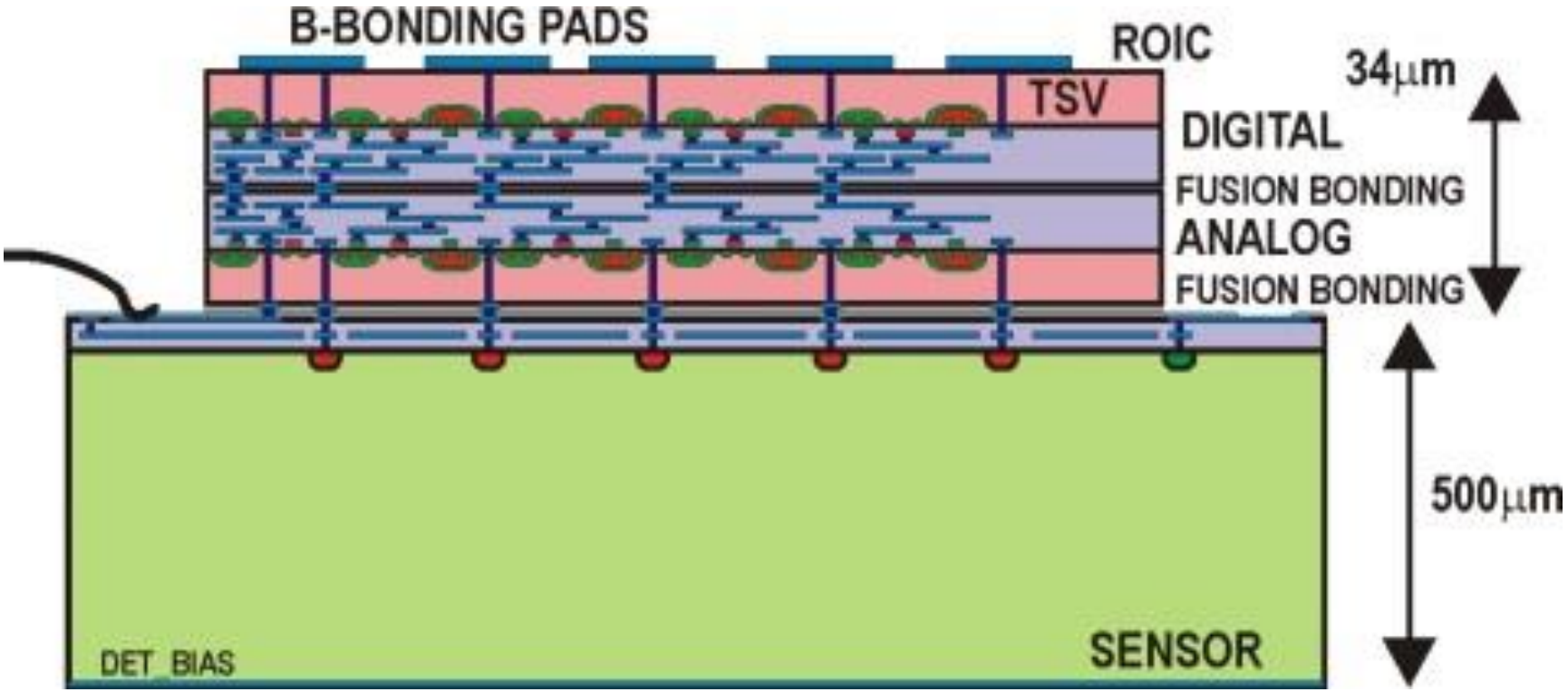
■ Figure 2 Sony's Objectives as an Image Sensor Supplier



http://www.sony.net/Products/SC-HP/cx_news/vol68/pdf/sideview_vol68.pdf#page=1

Demonstrator of 3D integration (G. Deptuch)

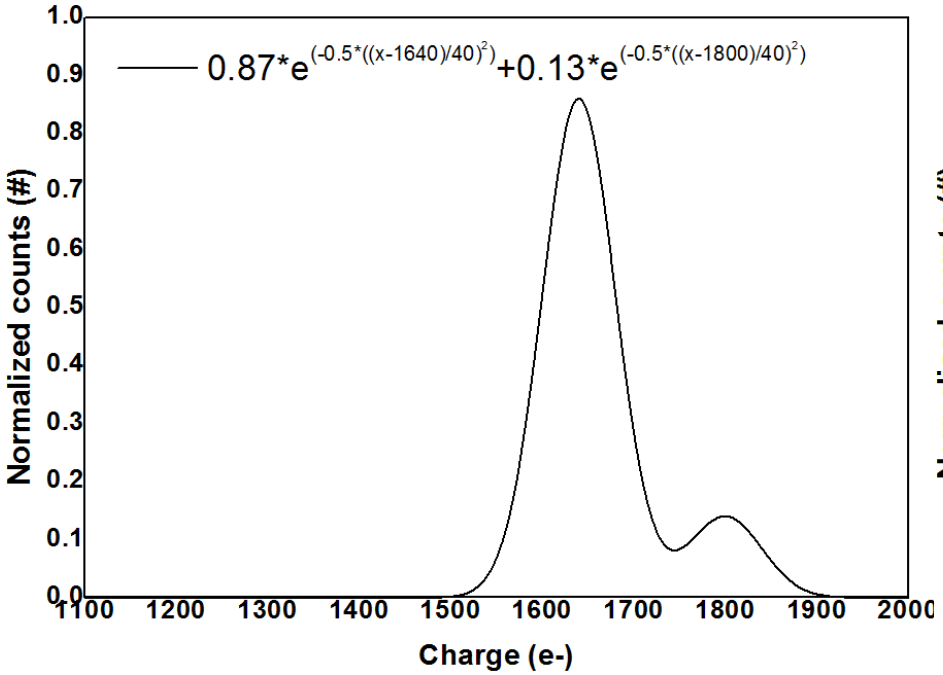
Vertically Integrated Photon Imaging Chip (VIPIC)
detector: Si d=500 μm, pitch 80×80 μm^2, soft 8keV X-rays
application: XPCS

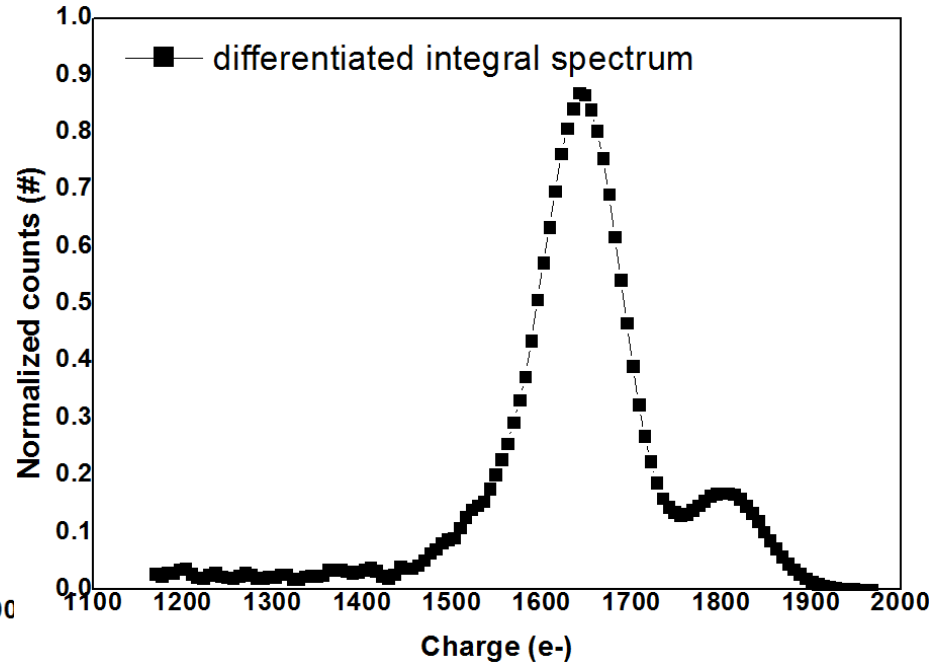


VIPIC bonded to sensor can be tested through wire bonded and bump-bonded connections

Can 3D integrated compete with MAPS?

NOISE





Sum of two Gaussian functions with:

x_{01}=1640 and σ_1=40

x_{02}=1800 and σ_2=40

Spectrum of ^{55}Fe with 500 μm thick, fully depleted (V_{dep}=170V) Si sensor,

(VIPIC1: 80 × 80 μm^2 pixel pitch, 64 × 64 pixels, with 150-200 ns shaping time

Summary

Status of sensors for future supercolliders: silicon (3d and planar hybrid pixels, microstrips) provides the required performances (with high demand in cooling and routing of the services).

Future requirements point very strongly on low mass, fast, high granularity sensors. This has strong implication on systems: reading out large numbers of channels in short times, small signals, minimise cooling requirements ..... The integration between sensor and electronics needs robust R&D: the small analogue signal cannot be driven over significant distances, they will require local processing. Electronics will have to provide this with limited power consumption!

Summary

The various integrated designs are advanced and are already baseline for several applications: DepFET (Belle), CMOS-MAPS (ALICE and others), HV-CMOS (Mu-3e). HV-CMOS in particular can be used in stand-alone or can be hybridised to readout electronics. It can offer much cheaper hybridisation (gluing instead of bump-bonding), and segmentation within a single readout channel (e.g. Analogue encoding). In this sense it is the technology that can replace hybrid pixels and micro-strip sensors for the HL-LHC, if radiation tolerance expectations are confirmed.

The 3D integrated sensor might be come available in future, but the progresses in this direction have been slower than expected.