Twepp 11

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Two areas of interest

Xilinx FPGA developments

Bio Inspired Image Processing.
Xilinx Series 7
Steve Trimberger, Xilinx Fellow
Xilinx 7 Series

• Xilinx 7 series, we are told, is very impressive.
• More than a bigger PLA with specialist area of silicon strapped to it.
• New Tech FPGA with specialised Silicon strapped to it.
• It is targeted at the commercial markets therefore,
Xilinx 7 Series

28 nm tech, 50% power reduction on 40 nm tech giving low power / heat per logical operation.

Artix
Bargain Chip

Kintex
Market Sweet Spot

Virtex
High End Cruncher
Capacity at 28 nm

![Bar chart showing the capacity at 28 nm for different FPGA types: Virtex-5, Spartan 6, Virtex-6, Artix-7, Kintex-7, Virtex-7. Virtex-7 has the highest capacity.](chart.png)
Agile Mixed Signal (AMS) Technology

General Purpose 12 analog ADC will be available on the 7 Series front end.

On board temperature and voltage monitoring

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# Transceiver Speed

<table>
<thead>
<tr>
<th>Transceiver type</th>
<th>Device</th>
<th>Rate Max Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>GT28</td>
<td>New 7 series</td>
<td>28</td>
</tr>
<tr>
<td>GTH</td>
<td>Virtex-7X</td>
<td>13.1</td>
</tr>
<tr>
<td>GTH</td>
<td>Virtex-6</td>
<td>11.18</td>
</tr>
<tr>
<td>GTX</td>
<td>Kintex -7</td>
<td>10.3125</td>
</tr>
<tr>
<td>GTX</td>
<td>Virtex-7 T</td>
<td></td>
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<tr>
<td>GTX</td>
<td>Virtex-6</td>
<td>6.6</td>
</tr>
<tr>
<td>GTP</td>
<td>Artix-7</td>
<td>3.75</td>
</tr>
<tr>
<td>GTP</td>
<td>Spartan-6</td>
<td>3.125</td>
</tr>
</tbody>
</table>
Processor Integration

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Processors

- Power PC hard processors will be replaced by a different architecture.
- Different approach in keeping with series 7 philosophy.
- ZYNQ 7 series
- Not a processor or and FPGA but something in between.
ZYNQ 7020

ZQ 7020
Processor:
ARM Cortex A9,
54 gpio, Standard peripherals,
73 DDR io etc.
Programable logic:
85K gates, 220 DSP blocks,
200 io, dual 12 bit ADC and
much more.
Auto Pilot
C, C++ or SystemC based configuration tool.
Removes the need to understand hardware description language

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For the Future?

- Xilinx are looking to produce market specific devices. We would be interested in telecoms and automation.

- Configuration tools are market lead and so will move from lower level description languages to greater levels of abstraction. C or C++.

```c
void core (
    int n; // input
    float* data_in1; // input data stream
    float* data_in2; // input data stream
    float* data_out // input data stream
){
    int i, j=0;
    for (i=0; i<n; i++)
        data_out[i] = data_in1[i] + data_in2[i];
}
```
Bio Vs Digital

Brains:
- Imprecise
- Error-prone
- Slow
- Flexible
- Concurrent
- Adaptive - tolerant of Component failure
- Autonomous learning

Computers:
- Precise
- Deterministic
- Fast
- Inflexible
- Serial
- Susceptive to single-point failure
- Program code
Current State of Electronics

- **Computer**
  - 0.0000000001 Joules / instruction (ARM968)
    - Chip: $10^{-11}$ J/operation
    - Computer system level: $10^{-9}$ J/operation

- **Brain**
  - Brain: $10^{-15}$ J/operation
Conventional Image Sensing

- Real time data is sliced into frames
- each pixel on the frame is recorded and processed.
- For still image data the information is processed using Discrete cosine transform to remove high frequency information that we are not aware of (JPG).
- For a moving image each JPG is compared to its neighbours and only the differences are recorded. To ensure movie stability, reference frames are inserted every so often. (mpeg-2)
Conventional Image Sensing

Single Frame Clock Cycle
Biological Approach

- **135 million** photoreceptors – detection threshold (rod): 1 photon
- **1 million** ganglion cells in the retina **process** visual **signals** received from groups of (few to several hundred) **photoreceptors**.
- Analog **gain control**, **spatial** and **temporal filtering**: ~ 36 Gb/s HDR raw image data is compressed into ~ 20 Mb/s spiking output to the brain
- Retina encodes **useful** spatial-temporal-spectral **features** from a redundant, wide dynamic range world into a small internal signal range.
- Power consumption: ~ 3.5 mW
Neuromorphic Dynamic Vision Sensor (DVS)

- Pixel has autonomous operation over clocked operation.
- Sensor is event driven change is recorded and not missed.
Conventional Image Sensing

Sensor → Data → Raw to Jpg conversion → Jpg to Mpg conversion

Single Clock Cycle
Conventional Image Sensing

Sensor

Event
Image Data Rates
Neuromorphic Dynamic Vision Sensor (DVS)

- Frame approach replaced with Eye-like function.
- Pixel responds to relative change rather than absolute threshold.
- Sensor is event driven change is recorded and not missed.
Image Data Rates
ATIS Pixel

ATIS Pixel

PD1

change detector

trigger

exposure measurement

change events

PWM grayscale events

time
So far I have..

• Polished 400 tonnes of lead 1 KM underground in a salt mine.
• Lived in a car park in CERN
• Spent over a year in a Nuclear Power station in Rice growing country in Japan.
• Visited Wheaton IL.
Transport
Entertainment
The Canteen